

METAL CONTACTS ON LOW-DIMENSIONAL MATERIALS

by

Hui Yuan
A Dissertation
Submitted to the
Graduate Faculty
of
George Mason University
in Partial Fulfillment of
The Requirements for the Degree
of
Doctor of Philosophy
Electrical and Computer Engineering

Committee:

_____ Dr. Qiliang Li, Dissertation Director
_____ Dr. Rao V. Mulpuri, Committee Member
_____ Dr. Dimitrios E. Ioannou, Committee Member
_____ Dr. Erhai Zhao, Committee Member
_____ Dr. Guangjun Cheng, Committee Member
_____ Dr. Curt A. Richter, Committee Member
_____ Dr. Monson H. Hayes, Department Chair
_____ Dr. Kenneth S. Ball, Dean, Volgenau School of Engineering

Date: _____ Fall Semester 2014
George Mason University
Fairfax, VA

Metal Contacts on Low-Dimensional Materials

A Dissertation submitted in partial fulfillment of the requirements for the degree of
Doctor of Philosophy at George Mason University

by

Hui Yuan

Bachelor of Engineering, Electronic Science and Technology, Wuhan University, 2006
Master of Science, Condensed Matter Physics, Wuhan University, 2009

Director: Qiliang Li, Professor
Department of Electrical and Computer Engineering

Fall Semester 2014
George Mason University
Fairfax, VA

Copyright 2014 Hui Yuan
All Rights Reserved

ACKNOWLEDGEMENTS

I would like to thank my friends and colleagues who have helped me to make this happen. My advisor, Prof. Qiliang Li, guided me in my research. My supervisor, Dr. Curt A. Richter, in National Institute of Standards and Technology, Gaithersburg, MD, helped me on many technical issues in my research. Dr. Guangjun Cheng taught me the research and analysis of the experiment data on MoS₂ materials. Also, I very much appreciate Professors Dimitrios E. Ioannou, Erhai Zhao, and Rao V. Mulpuri for their advice and help. Finally, my earnest thanks go to my parents who have supported me for all time.

TABLE OF CONTENTS

	Page
List of Figures	vi
Abstract	ix
Chapter 1: Background and Introduction.....	1
1.1 Emerging Applications of Low-Dimensional Materials in MOSFETs.....	1
1.2 Challenges in Metal Contacts on Low-Dimensional Materials	3
1.2.1 CMOS Scaling and SiNW Contact Characterization	4
1.2.2 Interface Impacts in MoS ₂ Metal Contacts.....	5
1.2.3 Current Crowding in Metal Contacts on MoS ₂	9
1.3 Overview of Dissertation.....	10
Chapter 2: Contact Characterization on Ambipolar SiNW FETs Based on Gate-assisted Kelvin Structure	12
2.1 Introduction	12
2.2 Contact Resistance Dependence on Electron Transport Direction in Ambipolar SiNW FET.....	13
2.2.1 Device Structure and Fabrication	14
2.2.2 Results and Discussion	17
2.2.3 Conclusion	23
2.3 Inverter on a Single SiNW	23
Chapter 3: Role of Interface Morphology on Metal Contacts to MoS ₂	28
3.1 Introduction	28
3.2 Experimental Methods	30
3.2.1 Sample Preparation:.....	30
3.2.2 Characterizations:	33
3.3 Results and Discussion.....	34
3.3.1 Electrical Characterization of MoS ₂ transistors.....	34
3.3.2 Surface Morphology of Metal Thin Films on MoS ₂	38

3.3.3 Raman Spectroscopy of MoS ₂ Covered with Metal	42
3.4 Conclusion.....	48
Chapter 4: Gate Effects and Current Crowding in Metal/MoS ₂ Contacts	49
4.1 Introduction	49
4.2 Experimental	51
4.3 Results and Discussion.....	54
Chapter 5: Summary and Prospectiv Future Plan	63
5.1 Summary of the Dissertation.....	63
5.2 Prospective Future Plan.....	64
Appendix A: Polarization of Bi ₂ Te ₃ Thin Film in a Floating-Gate Capacitor Structure. 66	
A.1 Introduction	66
A.2. Experimental	68
A.3 Results and discussion.....	70
A.4 Conclusion.....	78
References.....	79

LIST OF FIGURES

Figure	Page
Figure 1.1 Complications in metal contacts on MoS ₂ . (a) Schottky barrier height changes in experiment where metals with different Fermi levels are used. The Fermi level is pinned to the edge of conduction band. (b) MoS ₂ Fermi level changes after different metal contacts are applied in theoretical simulations. (c) I-V characteristics measured at different locations on a single piece of MoS ₂ with the tungsten probe directly contacting the MoS ₂	7
Figure 2.1 Fabrication process of SiNW transistors.	14
Figure 2.2 Device structure and measurement set-up. (a) Schematic of device structure and measurement set-up. (b) Scanning electron microscopic image of the SiNW gate assisted Kelvin test structure. Yellow circle shows the SiNW FET (channel length: 50 nm). The inset in (b) shows the magnified image of the yellow circled region. Scale bars in (b) and inset are 1 μm and 100 nm long, respectively.	15
Figure 2.3 Scheme of the cross section off the SiNW under S/D contacts.....	16
Figure 2.4 Electric characterization: (a) Ambipolar I _{DS} vs. V _{GS} characteristics. (b) Hole contact characteristics selected by negative V _{GS} . Electron contact characteristics selected by positive V _{GS} : (c) electrons flow from Al to the SiNW channel; (d) electrons flow from the SiNW channel to Al.....	18
Figure 2.5 Diffusion of Al in silicon: (a) Al concentration before annealing at 300°C for 30 minutes in O ₂ . (b) Al concentration after annealing at 300°C for 30 minutes in O ₂	21
Figure 2.6 Band diagram from channel center to the contact at different conditions: (a) Equilibrium state. (b) V _{DS} < 0 and V _{GS} < 0: hole flow from Al to SiNW. (c) V _{GS} > 0 and V _{DS} > 0: electrons flow from Al to SiNW (d) V _{GS} > 0 and V _{DS} < 0: electrons flow from SiNW to Al.....	22
Figure 2.7 SEM image and measure set-up of the inverter.....	25
Figure 2.8 Voltage transfer characteristics of single nanowire CMOS inverter under V _{DD} = 2 V and V _{IN} = 0~4 V.....	26
Figure 3.1 MoS ₂ flake on SiO ₂ /Si substrate. (a) AFM image of a MoS ₂ flake which includes monolayer, trilayer and multiple layer regions. (b) Optical image of the same flake. (c) Raman spectra of different thickness MoS ₂ which is collected from the different positions on the same flake of MoS ₂	31
Figure 3.2 MoS ₂ transistor diagram and Drain current density of single-layer MoS ₂ transistors: (a) MoS ₂ transistor diagram Drain current density of single-layer MoS ₂ transistors versus (b) V _G -V _{th} with Ag or Ti contacts, and (c, d) drain voltage (V _{DS}) with (c) Ag or (d) Ti contacts.	35

Figure 3.3 Drain current density of few-layer MoS ₂ transistors versus (a) V _G -V _{th} with Ag or Ti contacts, and (b, c) drain voltage (V _D) with (b) Ag or (c) Ti contacts.	37
Figure 3.4 SEM images of MoS ₂ on SiO ₂ /Si substrate after (a) Au / Ag deposition and (b) Au/Ti deposition. The insets show corresponding optical image of pristine MoS ₂ before metal deposition. The locations of monolayer MoS ₂ (1L) and few-layer MoS ₂ (FL) are identified after metal deposition.	39
Figure 3.5 AFM and roughness analysis of metal on MoS ₂ and SiO ₂ /Si substrate: (a) Topography of Au/Ag on MoS ₂ and SiO ₂ /Si. (b) A topographic line profile of the height along the slide line indicated in figure (a). (c) Normalized histograms of height distribution of areas indicated by the square in figure (a). (d) Topography of Au/Ti on MoS ₂ and SiO ₂ /Si. (e) A topographic line profile of the height along the slide line indicated in figure (d). (f) Normalized histograms of height distribution of areas indicated by the square in figure (c). Scale bars are 500nm long for image (a) and (d).	41
Figure 3.6 Comparison of Raman spectra before and after (a) Au/Ag or (b) Au/Ti deposition on monolayer (1L) MoS ₂ and before and after (c) Au/Ag or (d) Au/Ti deposition on few-layer (FL) MoS ₂ . The scatters are real data and solid lines are fitted Lorentz peaks.	42
Figure 3.7 Raman spectra on Au/Ti covered MoS ₂ with different power and signal collection time. Scatters are experimental data and solid lines are fitted curves. .	47
Figure 4.1 (a) System set-up for MoS ₂ CVD. (b) Image of typical MoS ₂ flakes grown on SiO ₂ /Si substrate. The scale bar is 5 μm. (c) Device schematic.	52
Figure 4.2 Device structure: (a) Schematics of MoS ₂ FETs (b) SEM image of a MoS ₂ transistor. Scale bar in this image is 1 μm.	54
Figure 4.3 I-V characterization of a representative MoS ₂ FET: (a) I _D -V _G , and (b) I _D -V _D characteristic.	55
Figure 4.4 Gate assisted Kelvin test: (a) V ₂₃ -I _D measured at different V _G , inset is the illustration of the measurement set-up; (b) R _{C-K} extracted from the linear fitting of V ₂₃ and I _D at different V _G	56
Figure 4.5 Gate assisted 4-probe measurement. (a) Channel sheet resistance at different V _G , inset is the measurement set-up for gate assisted 4-probe measurement. (b) Contact resistance (R _C) extracted from 4-probe measurement.	57
Figure 4.6 TLM model for contact resistance. The positions where the voltage is sampled in Kelvin method and 4-probe measurement are pointed.	58
Figure 4.7 (a) Current transfer length and (b) Contact resistivity at different V _G	61
Figure A.1 (a) Schematic of the capacitor with Al/Al ₂ O ₃ /Bi ₂ Te ₃ /SiO ₂ /Si structure. (b) High-resolution transmission electron microscopy (HRTEM) image of the capacitor cross-section. The scale bar is 5 nm in the image. The rectangular HRTEM image (10nm × 5nm) on the right is an amplification of the Bi ₂ Te ₃ film within the red rectangle on the left image, showing the polycrystalline structure in the film. (c) AFM image of Bi ₂ Te ₃ film grown on SiO ₂ with OH-hydroxyl groups by ALD.	69
Figure A.2 (a) Capacitance-Voltage (C-V) characteristics of the Bi ₂ Te ₃ capacitor structure at 1 MHz with different voltage sweep ranges. The area of the capacitor	

is $100\ \mu\text{m} \times 100\ \mu\text{m}$. (b) The polarization difference changes versus the applied voltage. (c) Illustration of the charge separation and polarization of Bi_2Te_3 when an external field is applied. 72

Figure A.3 C-V characteristics the Bi_2Te_3 capacitor structure at different frequencies (1 kHz to 1 MHz) at different temperatures: (a) 290K, (b) 280K, (c) 270K and (d) 250K. The hysteresis shift decreases as the temperature decreases..... 76

Figure A.4 (a) Polarization difference at vs. applied voltage different temperatures. (b) Memory window vs. temperature. The memory window is shrunk as the temperature decreases, indicating that the remnant polarization becomes smaller at lower temperature. The memory window is fitted as an exponential function of $1/k_B T$ ($k_B T$ is the thermal activation energy), agreeing well with both the linear- and log-scale experimental data. The activation energy is 0.33eV according to the fitting..... 77

ABSTRACT

METAL CONTACTS ON LOW-DIMENSIONAL MATERIALS

Hui Yuan, Ph. D.

George Mason University, 2014

Dissertation Director: Dr. Qiliang Li

As the scaling of the microelectronics is reaching nano regime, low-dimensional materials have been of increasing interest for future electronics applications. The low-dimensional materials, such as Si nanowires (SiNWs), carbon nanotubes (CNTs), graphene and transition metal dichalcogenides (TMDs), not only provide small body for further-scaled devices but also bring about new intrinsic properties for application in future optoelectronics, spintronics and so on. However, the small dimensions add significant difficulty for reducing contact resistance in the nanoelectronic devices. This dissertation presents a study of the metal contacts on low-dimensional materials. The focus of this work is on SiNWs and monolayer or few-layer MoS₂.

First, the metal contact on SiNW field effect transistors (FETs) was studied with a gate assisted Kelvin structure. In this work, I fabricated ambipolar SiNW FETs with Al contacts. The ambipolar characteristics and the gate assisted Kelvin structure enabled the

measurement of the contact properties of both electron and hole flows at the same contact. In this work I found that the contact performance is affected by the carrier type that flows in the channel as well as the current direction. In addition, an inverter was designed and realized on a single SiNW leveraged by the ambipolar FET characteristics.

Then, I have studied metal contacts on MoS₂, which is one of typical two-dimensional semiconductors. In the first part of this work, Ag and Ti contacts on exfoliated MoS₂ monolayers and few-layers are fabricated, characterized and analyzed. Based on the current-voltage (I-V) measurement, surface morphology and Raman spectroscopic measurement, I found that interface morphology plays an important role on the contact performance in MoS₂ FETs. In the second part of this work, gate-assisted contact measurement was carried out on chemical vapor deposited low-dimensional MoS₂ layers. The contact resistance and current crowding have been measured and analyzed at different gate bias. All these findings contribute to the understanding of metal contact on MoS₂.

SiNWs and MoS₂ are well-representative examples of emerging low-dimensional materials. The gate assisted contact measurement and metrology can also be applied to understand the metal contacts on other emerging low-dimensional materials.

CHAPTER 1: BACKGROUND AND INTRODUCTION

1.1 Emerging Applications of Low-Dimensional Materials in MOSFETs

As the dimensional scaling of the microelectronics is reaching the fundamental physical and economic limits, more and more low-dimensional materials have been studied for future applications. The representative materials include (but not limited to) semiconductor nanowires (NWs) [1-3], carbon nanotubes (CNTs) [4, 5], graphene [6-8] and transition metal dichalcogenides (TMDs) [9-11]. They not only provide a small body for further down-scaled device, but also bring about new physical properties to be integrated into future optoelectronics, spintronics and so on. The nanowires, such as Si nanowires (SiNWs), can be used in electronic devices for the application of 3-dimensional (3D) device morphology like FinFET [12] in current device technology. Others like III-V compound nanowires have been studied for future photonics applications. The small body with unique properties provides an excellent platform for down-scaling the devices to overcome the physical limit of the conventional 3-dimensional materials.

The surface roughness of ultra-thin body Si on insulator (UTSOI) becomes very large when the thickness approaches to 5 nm. Besides, the quantum confinement significantly enlarges the bandgap of Si when its thickness decreased to 5 nm and below. These situations limit UTSOI applications in further scaled electronics. Fortunately, 2-

dimensional (2D) semiconductors, such as TMDs [13-15] and black phosphorus, [16-18] have an intrinsic thin body with robust crystal structure. Their thickness is normally atomically thin (just couple of atom layers). But they still boast semiconducting properties with a scalable bandgap. In addition, the ultra-thin body and high mechanic strength of 2D materials are advantageous for the flexible and stretchable electronic devices. [19, 20] Also, in recent years, these devices gained much attention for medical applications.

Furthermore, the low-dimensional nature brings about attractive materials properties. For example, CNTs can be conductor or semiconductor according to their chirality. [4] The semiconducting CNTs have a high carrier mobility which is attractive for high-frequency applications. [21] Like CNTs, graphene also has a high mobility because carriers in graphene are the massless Dirac fermions. [22] It has also attracted intensive attention for high-frequency applications [8]. Graphene radio frequency (RF) devices with cutoff frequency (f_T) of 300 GHz have also been demonstrated. [23] The long spin coherence time exhibited by graphene makes it also an interesting material to be used in spintronics and quantum computing. [24-26]

Unlike the bulk TMDs which are indirect bandgap semiconductor, the monolayer TMDs are usually direct bandgap semiconductor. [27, 28] As a result, they are preferred for both electronics and optoelectronic devices. More recently, researchers demonstrated significant valley polarization in graphene [29, 30] and MoS₂. [31, 32] This physical property might bring about a new concept of valleytronics into devices.

1.2 Challenges in Metal Contacts on Low-Dimensional Materials

Though low-dimensional materials have above-mentioned advantages and prospective for future applications, the small dimensions place significant obstacles on achieving low contact resistance in the electronic devices. As stated in International Technology Roadmap for Semiconductors, 2013 Edition, contact resistance has a large impact on device performance as devices are scaled to smaller dimensions. [33] Theoretically, the contact resistance is determined by the energy alignment between the metal work function and the semiconductor bandgap. However, metal/semiconductor interface usually forms Schottky barrier. Its barrier height cannot be effectively tuned by the metal Fermi level because of Fermi level pinning. [34] In the past, the contact resistance can be reduced with heavily doped semiconductor. In this way, the width of the Schottky barrier at the metal semiconductor interface is greatly reduced so that the tunneling through the barrier is highly enhanced. However, this is not possible in many nanoscale devices as the doping is difficult to control at that small dimensions. In addition, the alloy formed at the contact between metal contacts and semiconductor would consume considerable channel thickness in a nanoscale multigate FET, (e.g., FinFET). Furthermore, for nanomaterial based devices such as carbon nanotube, graphene, or other 2D materials, reducing the barrier height is the only option since the material is extremely thin. Ideally, in order to obtain ultra-low-resistance contacts the metal work function should be aligned with the semiconductor Fermi level. However, Fermi level pinning often has a strong effect on the interface of metal/semiconductor contact. [35-38] Thus, metal Fermi level should not be the only consideration for low

contact resistance. Other factors of the contact interface should also be considered to achieve low contact resistance.

1.2.1 CMOS Scaling and SiNW Contact Characterization

As the dimensional scaling of conventional metal-oxide-semiconductor field effect transistors (MOSFETs) is approaching the fundamental limits, several device structures have been explored to further extend the functionality of complementary metal-oxide-semiconductor (CMOS) technology. [39] Among them, the most attractive devices are nanowire / nanotube field effect transistors (FETs), FinFETs and junction-less FETs.[12, 40-42] For thin, nanoscale sidewall contacts, the contact resistance can be very large and behave differently than in planar devices. The contact mechanism in one-dimensional (1D) electronic system [4, 43] and method to minimize contact resistance in Si nanowire transistors [44, 45] have been previously reported. However, proper contact characterization metrology is still an important and urgent issue in nanoelectronics. [41] For a nanoscale channel with low or even intrinsic doping, the resistance of the channel (e.g., ungated current < 1 fA) is too large for conventional measurements. The conventional transfer length method (TLM) [46] and Kelvin test structure [47] are no longer suitable. Also, the conventional cross-bridge Kelvin test structure cannot be fabricated on a one dimensional nanowire. In addition, the resistance of the nanoscale source/drain (S/D) contacts is quite different to the contact measured in the absence of gate electric field, which if present will affect the current crowding at the contact. [48] Furthermore, the extremely small device dimensions will introduce poor doping

uniformity, and the S/D asymmetry can be formed under sufficient bias. The conventional metrologies, such as TLM and 4-probe methods, cannot efficiently and precisely extract the contact resistance of a single contact. [49]

To meet these challenges, we designed a gate-assisted Kelvin test structure based on Si nanowire (SiNW) FETs to study the properties of nanoscale S/D contacts. With the SiNW FET based Kelvin test structure, we can select and measure the contact resistance (R_C) of a single contact. Also, we can investigate the contact characteristics for pure electron or hole flow at the same contact, and study the effect of carrier flow direction on the contact properties. We selected Si nanowires as a test platform, but the metrology can be applied to other nanoscale devices, such as nanotube FETs and FinFETs.

1.2.2 Interface Impacts in MoS₂ Metal Contacts

Recently, layered materials, such as MoS₂ and WSe₂, have attracted intensive attention for electronic and optoelectronic applications. [10, 11, 50-52] Monolayer and few-layer MoS₂ can be treated as 2-dimensional (2D) semiconductor. Their bandgap ranges from 1.2 eV to 1.8 eV depending on the number of layers. [14, 15, 27] In particular, monolayer MoS₂ has a direct bandgap of 1.8 eV, very attractive for applications in optoelectronics. [27, 53, 54] In addition, the 2D MoS₂ is attractive for flexible electronic applications because of its intrinsic ultrathin body and robust lattice structure. [19, 20, 55] In the consideration of short channel effects in metal-oxide-semiconductor field effect transistors (MOSFETs), the 2D intrinsic ultrathin body represents the ultimately small scale. [56] Moreover, its inert surface has no dangling

bonds, which is advantageous for forming the channel-gate dielectric interface in MOSFETs. Monolayer MoS₂ MOSFET was the first demonstrated 2D TMD semiconductor MOSFET. [9] Such transistors have exhibited a high ON/OFF ratio of 10⁸ and decent subthreshold slope of 74 mV/dec which are competent with state of art CMOS technology. [9]

Significant amount of work has been done to understand the transport mechanism in MoS₂ transistors and to improve their performance for future applications. [57-61] The Source/Drain (S/D) contacts are very important factors for device performance. Several contact structures have been used and studied to achieve a good Ohmic contact on MoS₂. [37, 38, 55, 62-64] It was expected that a metal with lower work function leads to a lower Schottky barrier for electron transport and results in a good n-type contact. [37]

However, the properties of metal contacts on MoS₂ is complicated and often suffers from Fermi level pinning which results in a Schottky barrier not fully tuned by the metal Fermi level. As shown in Fig. 1.1(a), the experimental results from S. Das et al. show that the barrier height between the MoS₂ channel and the metal contact is only weakly influenced by the metal work function and that an n-type barrier is formed between MoS₂ and a high work function metal such as Pt. [37] The theoretical work by C. Gong et al. confirms that partial Fermi level pinning in metal-MoS₂ contacts makes the Fermi levels in all studied metal-MoS₂ complexes except Pt are situated above the midgap of MoS₂, as shown in Fig. 1.1(b) [38] Additionally, S. McDonnell et al. demonstrated that intrinsic defects in MoS₂ dominated the metal-MoS₂ contact resistance and provide a low Schottky barrier independent of metal contact work function (Fig.

1.1(c)). [62] All above-mentioned results show that metal work function is not a good indicator for forming an Ohmic contact with MoS₂.

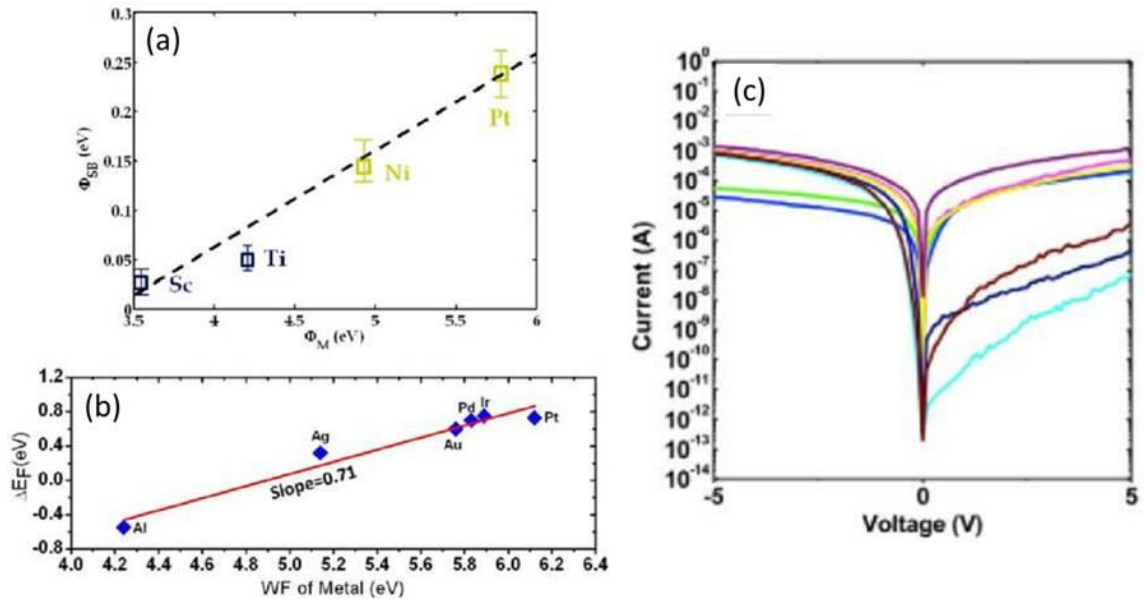


Figure 1.1 Complications in metal contacts on MoS₂. (a) Schottky barrier height changes in experiment where metals with different Fermi levels are used. The Fermi level is pinned to the edge of conduction band. (b) MoS₂ Fermi level changes after different metal contacts are applied in theoretical simulations. (c) I-V characteristics measured at different locations on a single piece of MoS₂ with the tungsten probe directly contacting the MoS₂

Previous studies on metal contacts to graphene or carbon nanotube indicated that the morphology of metal contacts and the interaction between these carbon-based materials and metal play important roles in contact resistance. [64, 65] Although it is well recognized that metal wettability plays an role in metal-MoS₂ contacts, [37] to our best knowledge, there is no work showing the direct evidence on how the metal contact

morphology affects the metal-MoS₂ contacts. In this work, for the first time, we have shown how the metal-MoS₂ interface influences the MoS₂ FET performance.

Ag was chosen because it has been reported to form a good contact on WSe₂, [66] which is a similar material to MoS₂. Previous work also shows that Ag has excellent wettability on bulk MoS₂. [67] We compare the results from Ag contacts with those from Ti contacts, which are commonly-used metal contacts on MoS₂ in the literature. [9, 37, 54, 68-71] Our results show that, despite of the similar work function around 4.3 eV for both metals,[72] monolayer and few-layer MoS₂ transistors with Ag contacts show significantly better electrical characteristics with more than 60-time higher ON-state current density and steeper subthreshold slopes.

The surface morphology of the metal films was then investigated. 5 nm thin layer of contact metal (Ag or Ti) capped with a 5 nm Au protection layer was deposited on top of MoS₂. Scanning electron microscopy (SEM) shows that Au/Ag formed a smoother and denser film on MoS₂. The surface roughness analysis was carried out by atomic force microscopy (AFM). The metal-MoS₂ interface was then investigated by Raman spectroscopy. The Raman spectra reveal that the contacting interface is between MoS₂ and Ag or Ti. The better wettability between Ag and MoS₂ is essential to form smoother and denser Au/Ag contacts on MoS₂, resulting in a better device performance. The strain effect introduced by Ag and heating effect introduced by Ti to monolayer MoS₂ are also revealed by the Raman spectroscopy.

1.2.3 Current Crowding in Metal Contacts on MoS₂

The current distribution under the metal contacts is an important property of the metal contacts. Some results show that the current would penetrate into the contact on a distance as large as several hundred of nanometers. [70, 73] However, their results are based on back-gated devices in which the channel current was not effectively tuned by the gate, and the Fermi level of MoS₂ under the contacts will be coupled to the back gate voltage. Here, we will present our work on the current crowding effect in metal-MoS₂ contacts which are affected significantly by a top gate. Our previous work shows that gate-assisted test structure is a good approach to test the contacts in low-dimensional electronic system. [74] We will extend the method to MoS₂ and do a cross comparison between Kelvin test structure and 4-probe method.

We fabricated Ag contacted bilayer MoS₂ transistors with 30 nm Al₂O₃ top gate on 300 nm SiO₂/Si substrate. The dimensions of our transistors are: 0.5 μm channel length, 4 μm channel width and 1 μm contact length. Ag was chosen because it has been reported to form a good contact on WSe₂, [66] which is a similar material to MoS₂. And our previous work shows Ag forms smooth and solid film on MoS₂ which makes the carrier transport efficiently across the contacts. Our devices show good n-type current-voltage (I-V) characteristics. Then gate assisted Kelvin structure and 4-probe method was used to analyze the contacts. The contact resistance extracted from the both methods is significantly different due to the difference in position where the voltage is sampled in each method. By comparing the contact resistance extracted from two methods, we found the current transfer length (L_T) of Ag-contact MoS₂ transistors is from 137 nm to 206 nm

(increased with the increasing gate voltage). The channel sheet resistance is measured by 4-probe method. It is much larger than the contact resistance which indicates that the MoS₂ transistors are channel dominant. The contact resistivity is then extracted from our data. It can be effectively tuned by the gate as well. Our result indicates that the gate affects the current crowding in the contacts, so as the contact resistivity.

1.3 Overview of Dissertation

In this dissertation, I will first present my work on the characterization of metal contacts on SiNW field effect transistors (FETs). In this work, metal contacts on SiNW FETs were studied with a gate assisted Kelvin structure. The SiNW devices were fabricated from chemical vapor deposited (CVD) SiNWs with conventional lithographic approaches. Al was used to form source/drain (S/D) contacts to SiNW transistors. The transistors exhibit ambipolar characteristics. The application of gate assisted Kelvin structure enabled the measurement of the contact characteristics of both electron- and hole-flow at the same contact. In this work, we found that the contact performance is affected by the carrier type that transport in the channel and also by the current transport direction. Also, based on the ambipolar characteristics of the transistors, an inverter was fabricated on a single SiNW.

Then, I will present an analysis of metal contacts on MoS₂, which is a 2D semiconductor. This work is divided into two parts. In the first part of this work, Ag and Ti contacts on exfoliated MoS₂ films are compared. Based on the current-voltage (I-V) measurement, surface morphology and Raman spectroscopy, I found interface

morphology plays an important role on the contact performance in MoS₂ FETs. In the second part of this work, gated assisted contact measurement was carried out on CVD MoS₂ transistors. The contact resistance and current crowding were measured and analyzed under different gate bias. Our results show that the gate voltage influences both contact resistivity and transfer length of the contacts. This indicates that contact resistance changes with gate voltage. This work also indicates that in our MoS₂, the contacts play an important role in device performance. All these findings contribute to understanding the metal contact mechanism on MoS₂ as well as the MoS₂ transistor performance.

Finally, a brief summary of my work on the metal contacts is drawn and future plan of this work is laid out. It should be pointed out that although SiNWs and MoS₂ are good examples for low-dimensional materials, the gate assisted contact measurement can be applied on other emerging low-dimensional materials. The contact characterization metrology discussed in this thesis is very useful to many other applications such as in light emitting diode (LED) and photovoltaic devices where contacts are important.

CHAPTER 2: CONTACT CHARACTERIZATION ON AMBIPOLAR SINW FETS BASED ON GATE-ASSISTED KELVIN STRUCTURE

2.1 Introduction

In this work, a gate assisted Kelvin test structure based on Si nanowire field effect transistors has been designed and fabricated for the characterization of the transistor source/drain contacts. Because the Si nanowire field effect transistors exhibit ambipolar characteristics with electron current slightly lower than the hole current, we can select the type of carriers (electrons or holes) flowing through the same contacts and adjust the current by the applied gate voltage. With this method, we are able to measure the characteristics of the same contact with either pure electron or hole flow. In addition, we found that the nanowire contacts behave very differently depending on the current flow directions. This indicates that the source and drain contact resistance can be dramatically different. Such a gate assisted Kelvin Test structure will lead to future metrology and applications in nanoelectronics.

Then, an inverter based on ambipolar Si nanowire FETs was integrated on to a single SiNW. The inverter is consisted of two identical nanowire FETs on a single Si nanowire. The engaged FETs showed asymmetric ambipolar characteristics under positive and negative gate bias. A CMOS-like inverter can be realized on the single

nanowire, where one of the devices behaves as an nMOSFET and the other behaves as a pMOSFET.

2.2 Contact Resistance Dependence on Electron Transport Direction in Ambipolar SiNW FET

In this work, a gate assisted Kelvin test structure based on Si nanowire (SiNW) FETs has been designed and fabricated to study the properties of nanoscale S/D contacts. Although a Kelvin test structure based on planar MOSFETs has been previously reported,[75] the three-dimensional nanoscale contact presents an exciting challenge. With this SiNW FET based Kelvin test structure, we can select and measure the contact resistance (R_C) of a single contact. We can also investigate the contact characteristics for pure electron or hole flow, and study the effect of carrier flow direction influencing on the contact behavior. We selected Si nanowires as a test platform, but the metrology can be applied to other nanoscale devices, such as nanotube FETs and FinFETs.

2.2.1 Device Structure and Fabrication

The fabrication process can be summarized in Fig. 2.1.

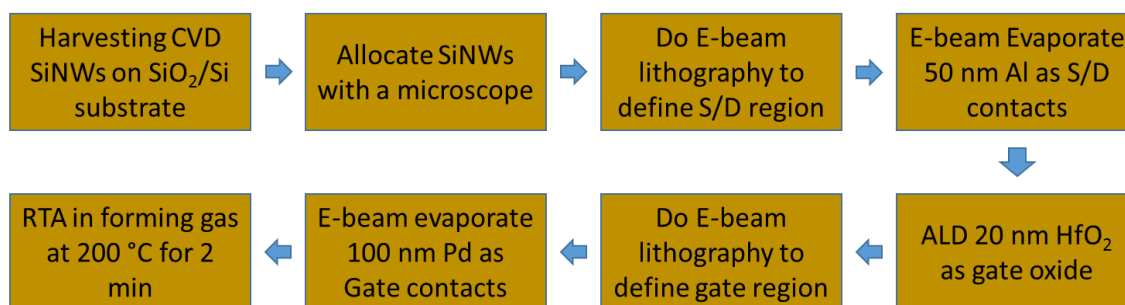


Figure 2.1 Fabrication process of SiNW transistors.

For the device reported here, the SiNWs were grown from Au catalyst by low pressure chemical vapor deposition (LPCVD) with SiH₄ as precursor. The SiNWs were grown at 450 °C for 2 hours with SiH₄ partial pressure of 500 mTorr. The resulting nanowires are in <111> orientation with an average diameter of the nanowires is 50 nm.

Then, the nanowires were harvested into methanol and dispersed on a Si substrate with 300 nm thermal SiO₂. The nanowires were oxidized at 750 °C to grow ≈ 2nm SiO₂, followed by e-beam lithography and metal formation. The S/D contact metal is Al of 1 μm width and 50 nm thickness. The gate/dielectric stack consists of 100 nm Pd on 20 nm HfO₂, deposited by atomic layer deposition (ALD) at 300 °C. The samples were then annealed at 200 °C in forming gas for 2 minutes to improve the interface and metal

contacts. In the test structure, there are three identical contacts on a single SiNW, separated by two short channels (50 nm long) sharing a common gate.

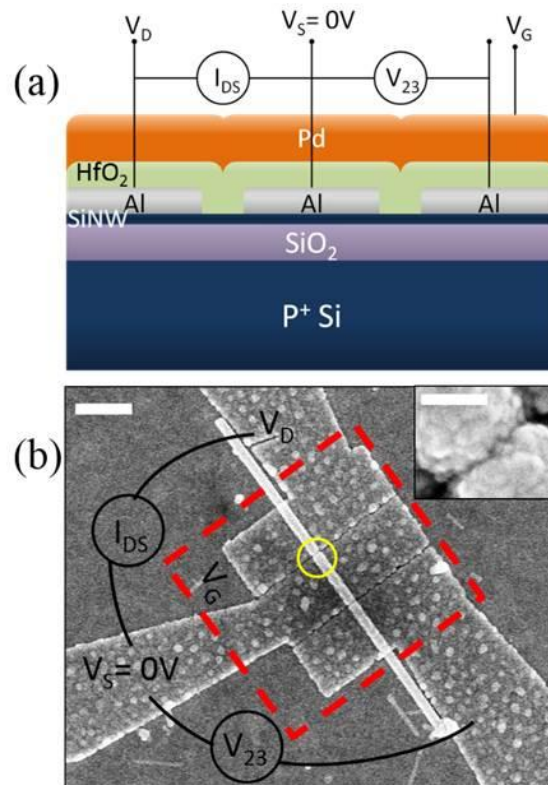


Figure 2.2 Device structure and measurement set-up. (a) Schematic of device structure and measurement set-up. (b) Scanning electron microscopic image of the SiNW gate assisted Kelvin test structure. Yellow circle shows the SiNW FET (channel length: 50 nm). The inset in (b) shows the magnified image of the yellow circled region. Scale bars in (b) and inset are 1 μm and 100 nm long, respectively.

As shown in Fig. 2.2, the gated Kelvin test structure consists of two SiNW FETs, sharing a common source, on a single nanowire. The resulting device scanning electron

microscopic (SEM) images and test setup is shown in Fig. 2.2. Even after the gate dielectric and contact formation, the position of the SiNW is still clear.

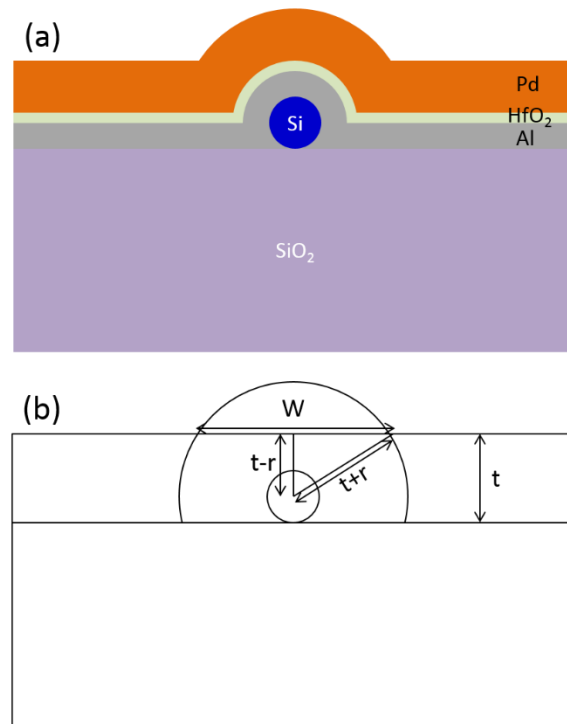


Figure 2.3 Scheme of the cross section off the SiNW under S/D contacts.

However, the dimension, especially diameter of the nanowire is obscured by the top layers. The width of the brighter pattern (202 nm in width) measured under SEM should be larger than the real diameter of the nanowire. As illustrated in Fig. 2.3(a), the measured width (W) is the width of the protrude region where the Si nanowire is covered by layers of Al, HfO₂ and Pd, totally 170 nm ($\approx 50\text{nm Al} + 20\text{nm HfO}_2 + 100\text{nm Pd}$). The width (W) in SiNW SEM image is not the SiNW diameter. The radius (r) can be

calculated following the schematic shown in Fig. 2.3(b), where t is the total thickness of the covering layers (170 nm).

The correlation between W and the radius of the Si nanowire can be estimated as:

$$\left(\frac{W}{2}\right)^2 + (t - r)^2 = (t + r)^2, \quad (1.1)$$

$$r = W^2/16t. \quad (1.2)$$

Therefore, the radius (r) and diameter of the Si nanowire are 15 nm and 30 nm, respectively. We drew this schematic of the cross section based on the cross section transmission electron microscopy (TEM) image of our previous devices. [76] The value of estimated diameter is quite consistent with our previous experiment where we used the same conditions to grow Si nanowires. [76]

2.2.2 Results and Discussion

The non-local voltage, V_{23} (Fig. 2.1) between the middle (2, the source: S) and one of the side contacts (3) is measured while a current (I_{DS}) is forced between the middle (2) and the other side contact (1, the drain: D), and thus the resistance of the middle contact is given by $R_C = V_{23}/I_{DS}$.

Fig. 2.4 shows the electrical measurements obtained with the above gate assisted Kelvin test structure. Fig. 2.4 (a) shows the drain current (I_{DS}) vs. gate voltage (V_{GS}) of the SiNW FETs at two source-to-drain voltage (V_{DS}) values. The SiNW FETs exhibit short-channel FET behavior with ambipolar characteristics. The electron current (positive V_{GS}) is lower than the hole current (negative V_{GS}). We did not intentionally dope the

SiNWs, therefore, the ambipolar behavior arises from the S/D contact properties. We believe the SiNW surface at the S/D contacts was doped p-type by Al diffusion during ALD of gate dielectric and these S/D junctions favor hole over electron flow (just one dopant atom in such a small nanowire body would be significant). [77]

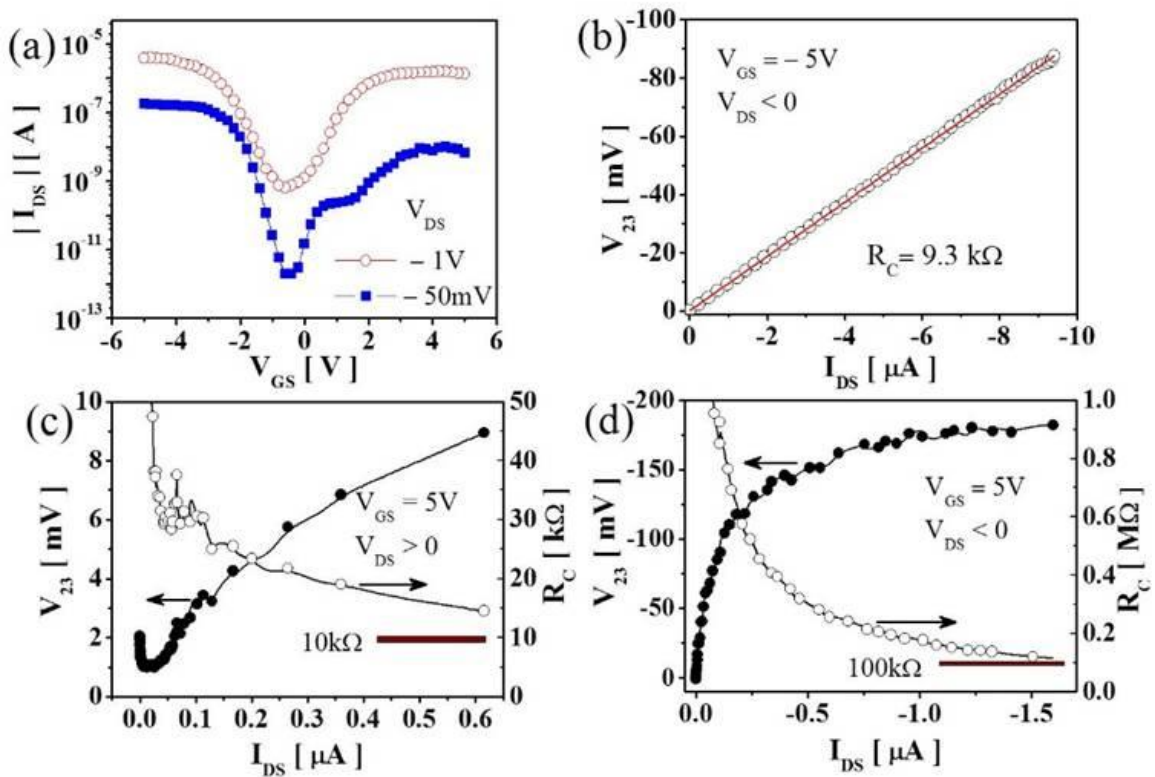


Figure 2. 4 Electric characterization: (a) Ambipolar I_{DS} vs. V_{GS} characteristics. (b) Hole contact characteristics selected by negative V_{GS} . Electron contact characteristics selected by positive V_{GS} : (c) electrons flow from Al to the SiNW channel; (d) electrons flow from the SiNW channel to Al.

To verify this, the electrical characteristics of the contacts are measured with the help of the gate assisted Kelvin test structure. Fig. 2.4(b) shows V_{23} versus I_{DS} at $V_{GS} = -5.0$

V (hole current) is linear, indicating the contact is Ohmic. The slope of the line shows $R_C \approx 9.3 \text{ k}\Omega$. For a Si nanowire of 30 nm in diameter and the contact of 1 μm in length, the specific contact resistivity for holes is thus $\rho_C \approx 8.8 \times 10^{-6} \Omega \cdot \text{cm}^2$. This specific contact resistivity is estimated by $\rho_C = R_C A$, where A is the contact area. (A is estimated to be $\pi D l$, where D is the diameter of the nanowire and l is the length of the contact.) [78] Fig. 2.4 also shows the contact resistance R_C for electron conduction from the SiNW to Al (Fig. 2.4(c)) and from Al to the SiNW (Fig. 2.4(d)), respectively. As expected for this contact, the resistance for electron flow (e-flow) is larger than that for hole flow (h-flow) and exhibits diode-like current-voltage behavior. It is interesting to see that R_C depends on the e-flow direction. The R_C value for e-flow from Al to SiNW decreases with increasing I_{DS} and approaches the hole R_C at large I_{DS} . But the R_C value for e-flow from SiNW to Al is >10 times larger than the hole contact resistance. Such difference due to carrier flow direction is not seen in the h-flow contact resistance in these devices. The value of contact resistance and contact resistivity extracted by this gate assisted Kelvin structure can be much smaller than the value extracted by TLM method. [79] However, the distinct behavior of the contact responding to h- and e-flow is clearly seen. Especially for e-flow, the contact characteristics exhibit a diode-like pattern. The contact behaves significantly different depending on different carrier transport direction. It should be noted that the R_C dependence on e-flow direction indicates the asymmetry in source and drain contacts. The contact we tested is source contact for the e-flow from Al to SiNW, while it is drain contact for the e-flow from SiNW to Al. According to our I_{DS} - V_{GS} characteristics, under a sufficient drain voltage $|V_{DS}| = 1 \text{ V}$, for the e-flow, the voltage

drop is $\approx 2\%$ or $\approx 30\%$ on this contact when it acts as source or drain contact respectively. Hence, from our results, R_C of drain contact is much higher (> 10 times) than that of source even if both contacts have identical physical characteristics. The conventional contact resistance characterization methods, such as TLM and 4-point measurement, cannot separate electron and hole flows or tell the difference between carrier flow directions.

The different contact behavior between h-flow and e-flow can be understood by the effects introduced by Al diffusion in Si. SiNW under the contact was doped into p-type because of the Al diffusion during the fabrication process. So that an Ohmic contact is expected for h-flow and a diode-like performance expected for the e-flow. To evaluate Al diffusion, we simulated Al diffusion in Si by using TCAD Sentaurus. Fig. 2.5 compares the Al concentration in the device before and after annealing. We generate a square Si nanowire with a high concentration of Al on the surface (Fig. 2.5(a)). The diameter of the Si nanowire is 50 nm. Our result shows after annealing the nanowire at 300 °C in O₂ ambient for 30 minutes sufficient Al diffused from surface into the Si (Fig. 2.5(b)). Like boron diffusion, O₂ enhancement of the Al diffusion is essential for the diffusion to happen at this low temperature. [80, 81] As O₂ plasma instead of H₂O was used as oxidant in ALD, it is reasonable to believe Al diffusion happened in our SiNW FET S/D contact.

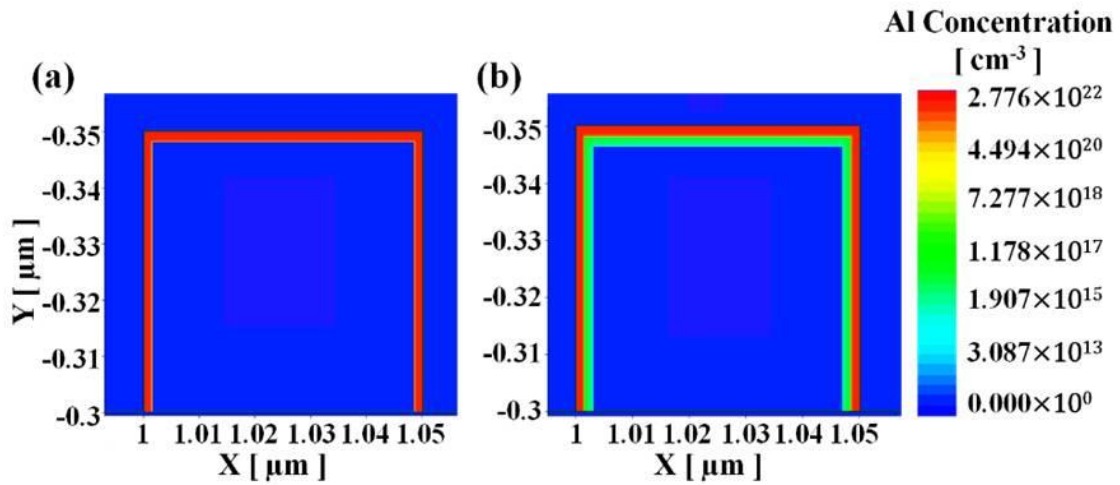


Figure 2. 5 Diffusion of Al in silicon: (a) Al concentration before annealing at 300°C for 30 minutes in O₂. (b) Al concentration after annealing at 300°C for 30 minutes in O₂.

Based on the doping concentration obtained from the diffusion simulation, the SiNW band diagram on the source contact adjacent under various bias conditions is generated by Sentaurus (see Fig. 2.6). The band bending is effectively tuned by V_{GS} . At negative V_{GS} , holes transport through the channel. It is clear an Ohmic contact is formed between channel and the source (Fig. 2.6(b)). At positive $V_{GS} = 5.0$ V, when $V_{DS} = 1$ V, electrons flow from Al contact to the SiNW channel (Fig. 2.6(c)), and vice versa for $V_{DS} = -1$ V (Fig. 4d). The electrons going down the hill (Fig. 2.6(c)) will experience less resistance than the electrons climbing up the barrier hill to reach the Al contact (Fig. 2.6(d)). We believe that the R_C for electrons flow from Al to SiNW at large I_{DS} and the hole R_C represents the net contact resistance excluding the effect of junction below the contact. This result proves that the gate assisted Kelvin test structure based on nanoscale FETs can measure not only the R_C of high resistance materials, but also the net R_C for both

Ohmic and diode-like contacts because it can separate and select the electron and hole flow.

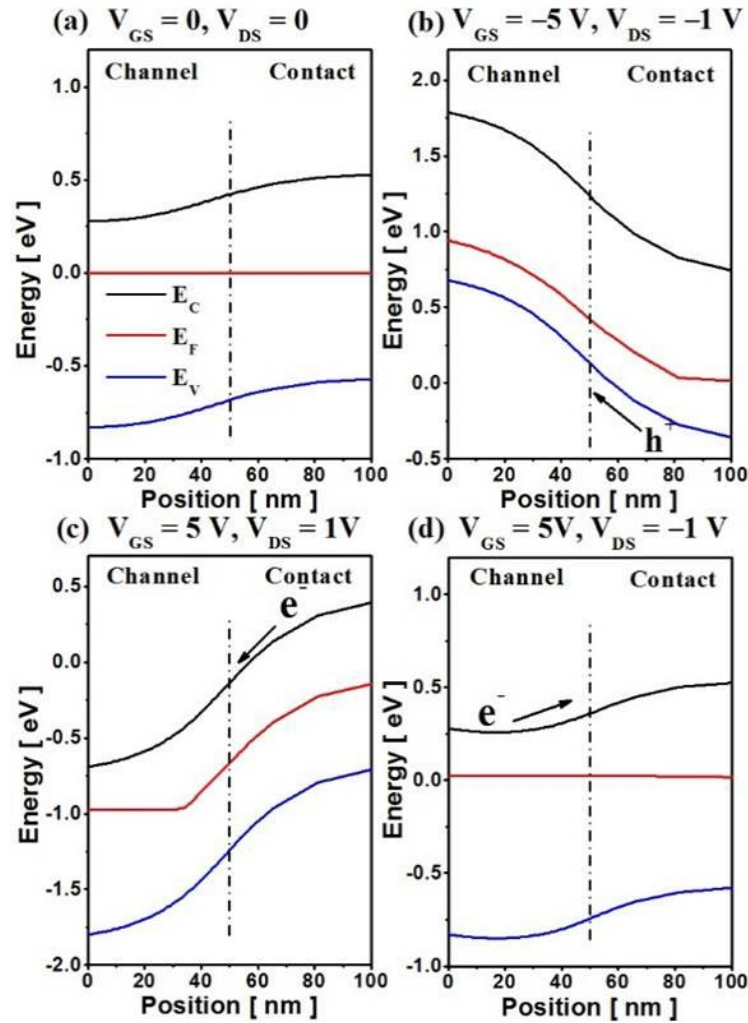


Figure 2.6 Band diagram from channel center to the contact at different conditions: (a) Equilibrium state. (b) $V_{DS} < 0$ and $V_{DS} < 0$: hole flow from Al to SiNW. (c) $V_{GS} > 0$ and $V_{DS} > 0$: electrons flow from Al to SiNW (d) $V_{GS} > 0$ and $V_{DS} < 0$: electrons flow from SiNW to Al.

2.2.3 Conclusion

In summary, we have designed and fabricated the gate assisted Kelvin test structure based on SiNW FETs. This test structure can efficiently detect the properties of electron and hole flows at the same nanoscale contacts. It has been found that the electron and hole flow resistances are very different; and the non-Ohmic contact resistance has a strong dependence on current direction. Also, the asymmetry between the source and drain contacts in a nanoscale FET can be determined by the gate assisted structure. Such an interesting gate assisted Kelvin test structure will lead to expand characterization metrology and may have important applications in nanoelectronics.

2.3 Inverter on a Single SiNW

As the scaling of Complementary Metal-Oxide-Semiconductor Field Effect Transistor (CMOS FET) continues, the challenge of short-channel effects (SCE) and exponentially increasing cost has almost become an impossible task for conventional bulk-Si based CMOS technology. [82] Several novel channel materials such as III-V compounds and graphene, and device structures including multi-gate and FinFETs were investigated to achieve better device performance like extended high frequency response or lower subthreshold slope. Among these candidates, Si nanowire (SiNW) is the most attractive channel materials for future CMOS FET due to its intrinsic semiconductor properties, small dimension and fully CMOS compatibility. We have been engaged in the research of bottom-up Si nanowire FETs with gate-all-around (GAA) structure for high performance. [76, 83] GAA structure provides excellent electrostatic gate control over transistor

channel even when channel length down to below 10 nm. [82] The SiNW based electronics built on a bottom-up self-assembly will have the advantage of low cost and high density.

However, the difficulties in controlling the doping level of SiNW make it too complicated to make traditional FETs with n-p-n or p-n-p doping structure. [2, 3] SiNWs with Schottky contacts (also indicated as Schottky barrier FETs) were demonstrated that they can work as enhancement-mode FETs. [43] In this case, the drain current level depends on the contact metal work function. The different conduction mechanisms for accumulation- and inversion-mode operation make it possible to make FETs with ideal ambipolar characteristics, so that an inverter can be integrated onto just one single nanowire with two identical MOSFETs one of which works as pMOS and the other as nMOS. In this work, we have designed a single-nanowire CMOS inverter based on ambipolar SiNW FETs with 50 nm channel length which we used in gate assisted Kelvin contact characterization.

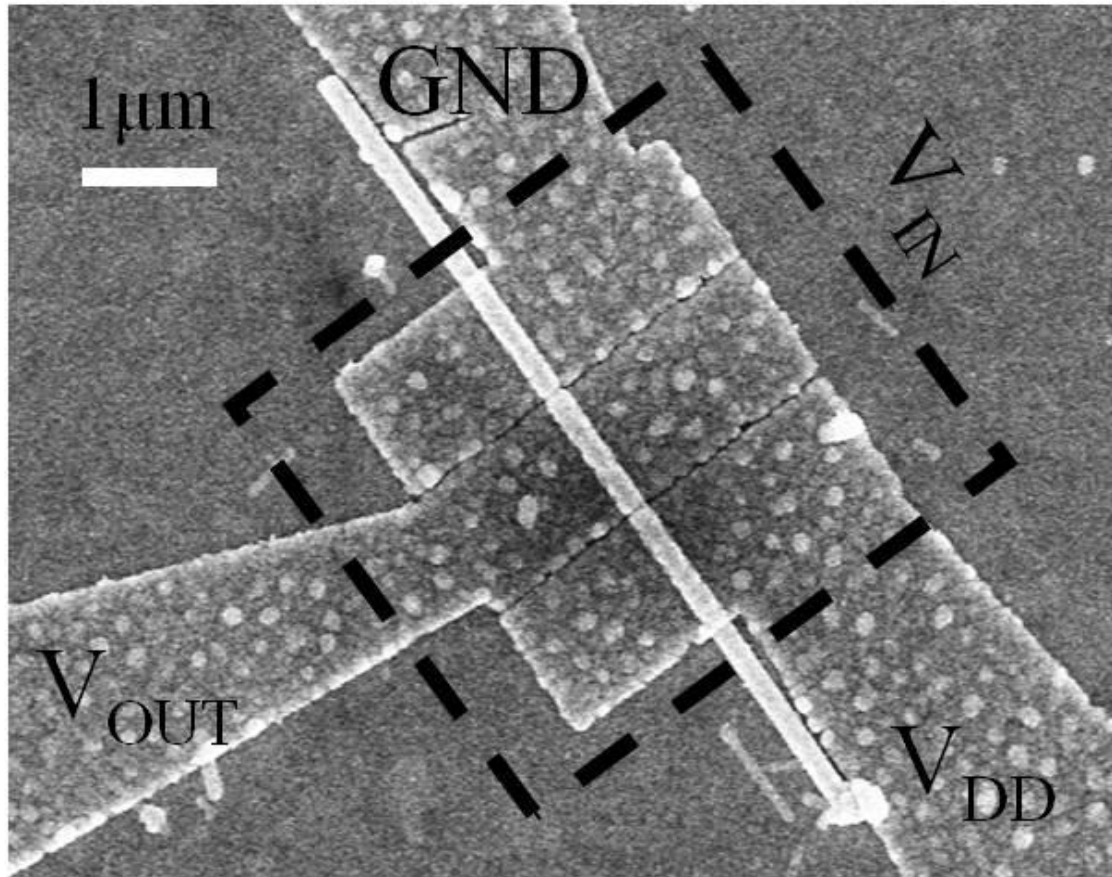


Figure 2. 7 SEM image and measure set-up of the inverter

The fabrication process and device structure are the same as previous SiNW FETs we used in contact characterization. The measurement set-up is illustrated in SEM image Fig. 2.7. The ambipolar I-V characteristics of the transistors inspired the possibility of fabricating CMOS logic gates using these SiNW FETs. A CMOS inverter based on two identical ambipolar SiNW FETs with 50-nm channel length built on one single nanowire (see Fig. 2.4). We measured the device with voltage supply (V_{DD}) of 2 V, and swept the input voltage from 0 to 4V (Fig. 2.8). The voltage transfer curve is slightly asymmetry in

this input range, but has small noise margin. The transfer happens mostly from 1V to 3V. So if we bias the input voltage to around 2V, we can get a symmetric output in a 2V input range from (2-1) V to (2+1) V.

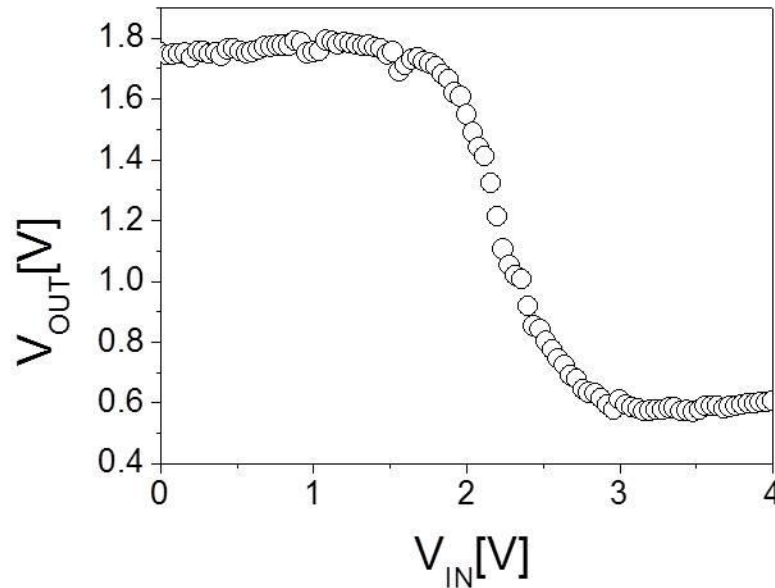


Figure 2.8 Voltage transfer characteristics of single nanowire CMOS inverter under $V_{DD} = 2$ V and $V_{IN} = 0\sim 4$ V.

The inverter works properly with slightly asymmetric behaviors and a small noise margin in voltage transfer. These issues can be resolved by engineering the threshold voltages and decreasing off-state current. In addition, the inverter has a very simple and yet very efficient structure. Various logic gates based on ambipolar SiNW FETs can be fabricated in two lithographic steps. Due to the scalability of nanowires and the

advantage of bottom-up process, this approach can lead to low-cost, high-density nanoelectronics circuitry.

CHAPTER 3: ROLE OF INTERFACE MORPHOLOGY ON METAL CONTACTS TO MoS₂

3.1 Introduction

Recently, MoS₂ has attracted a lot of attention for electronic and optoelectronic applications. [10, 11, 50-52] Layered MoS₂ is a 2-dimensional (2D) semiconductor which has a bandgap ranging from 1.2 eV to 1.8 eV depending on its thickness. [14, 15, 27] In particular, monolayer MoS₂ with a direct bandgap of 1.8 eV shows promising applications in optoelectronics. [27, 53, 54] 2D MoS₂ is also attractive for flexible electronic applications because of its intrinsic ultrathin body, and robust lattice structure.[19, 20, 55] Considering short channel effects in metal-oxide-semiconductor field effect transistors (MOSFETs), this intrinsic ultrathin body also represents the ultimate in scaling. [56] Moreover, its inert surface has no dangling bonds, which is advantageous for forming the channel-gate dielectric interface in MOSFETs. Monolayer MoS₂ MOSFET was the first demonstrated 2D TMD semiconductor MOSFET. [9] Such transistors have exhibited a high ON/OFF ratio of 10⁸ and decent subthreshold slopes of 74 mV/dec which is compatible with current state of art CMOS technology.

Various work has been done to understand the transport mechanism in MoS₂ transistors and to improve their performance for future applications. [57-61] The Source/Drain (S/D) contacts are very important factors for device performance. A variety

of contacts have been used and studied to achieve a good Ohmic contact on MoS₂. [37, 38, 55, 62-64] It was originally expected that a low work function metal may lead to a lower Schottky barrier for electron transport and result in a good n-type contact. [37] However, the experimental results from S. Das et al. show that the barrier height between the MoS₂ channel and the metal contact is only weakly influenced by the metal work function and that an n-type barrier even forms between MoS₂ and high-work function metal such as Pt. [37] The theoretical work by C. Gong et al. confirms that partial Fermi level pinning in metal-MoS₂ contacts makes the Fermi levels in all studied metal-MoS₂ complexes except Pt are situated above the midgap of MoS₂. [38] Additionally, S. McDonnell et al. demonstrate that intrinsic defects in MoS₂ dominate the metal-MoS₂ contact resistance and provide a low Schottky barrier independent of metal contact work function. [62] All these complications show that metal work function is not a good indicator for forming an Ohmic contact with MoS₂.

Previous studies on metal contacts to graphene or carbon nanotube demonstrate that the morphology of metal contacts and the interaction between these carbon materials and metal contacts play important roles in contact resistance. [64, 65] Although it is well believed that metal wettability plays an important role in metal-MoS₂ contacts, [37] to our best knowledge, there is no work showing the direct evidence on how the metal contact morphology affects the metal-MoS₂ contacts. In this work, for the first time, we have shown how the metal-MoS₂ interface influences the MoS₂ FET performance.

Ag was chosen because it has been reported to form a good contact on WSe₂, [66] which is a similar material to MoS₂. Previous work also shows that Ag has excellent

wettability on bulk MoS₂. [67] We compare the results from Ag contacts with those from Ti contacts, which are commonly-used metal contacts with MoS₂ in the literature. [9, 37, 54, 68-71] Our results show that, despite of the similar work function around 4.3 eV for both metals, [72] mono- and few-layer MoS₂ transistors with Ag contacts show significantly better electrical characteristics with more than 60-time higher ON-state current density and steeper subthreshold slopes.

The surface morphology of the metal films was then investigated by depositing 5 nm thin layer of contact metal (Ag or Ti) capped with a 5 nm Au protection layer on top of MoS₂. Scanning electron microscopy (SEM) shows that smoother and denser Au/Ag film is formed on top of MoS₂. The surface roughness analysis was carried out by atomic force microscopy (AFM). The metal-MoS₂ interface was then investigated by Raman spectroscopy and the Raman spectra reveal that the contacting interface is between MoS₂ and Ag or Ti. The better wettability between Ag and MoS₂ is essential to form smoother and denser Au/Ag contacts on MoS₂, resulting in a better device performance. The strain effect introduced by Ag and heating effect introduced by Ti to monolayer MoS₂ are also revealed by the Raman spectroscopy.

3.2 Experimental Methods

3.2.1 Sample Preparation:

The sample preparation starts with exfoliating bulk MoS₂ (SPI[®] small crystals) into mono- and few-layer films on 280nm SiO₂ / Si. The MoS₂ film thickness was confirmed by the color, Raman spectroscopy and AFM. (Figure 3.1) As seen in Figure

3.1(c), the distance between the two characteristic Raman peaks increases as the thickness of MoS₂ increases. This trend has been published repeatedly and widely accepted as a method to determine MoS₂ film thickness when it is only a few layers thick.[84] This thickness is also compared to AFM results to set a reference to identify MoS₂ thickness.

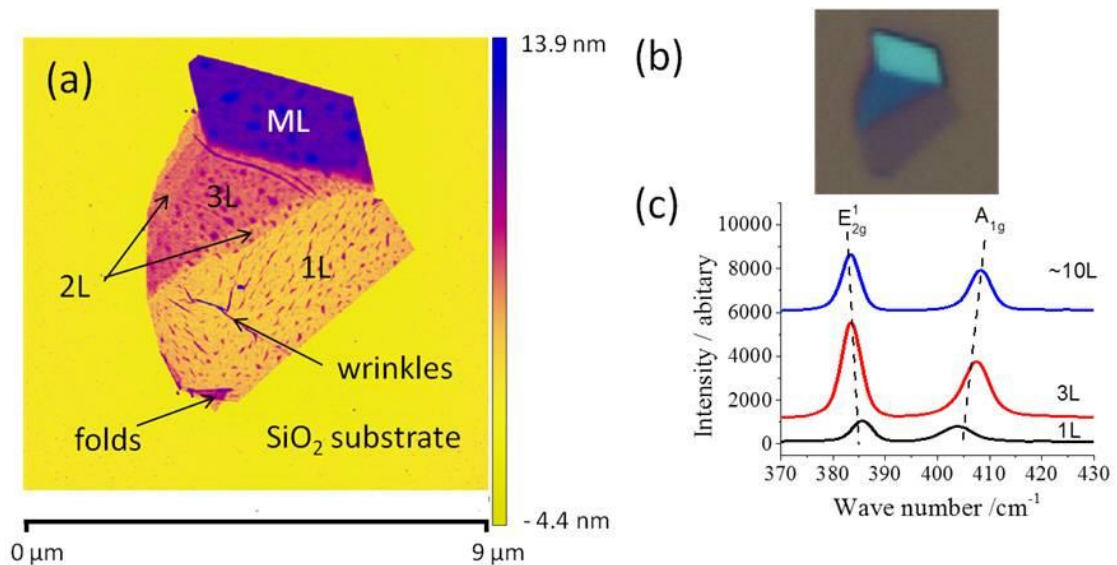


Figure 3.1 MoS₂ flake on SiO₂/Si substrate. (a) AFM image of a MoS₂ flake which includes monolayer, trilayer and multiple layer regions. (b) Optical image of the same flake. (c) Raman spectra of different thickness MoS₂ which is collected from the different positions on the same flake of MoS₂.

Then the back-gated mono- and few-layer MoS₂ transistors were fabricated for electric measurement. The detailed fabrication process is as following.

1. The MoS₂ flake positions are identified with pre-designed alignment marks by an optical microscope.

2. Pattern the source/drain contacts with electron-beam lithography. 495 PMMA A4 resist was used as resist. The resist was coated by spinning it onto the substrate at rotation speed of 3000 rpm for 45 sec. Then the substrate was heated on a hot plate at 180 °C for 2 min. The accelerate voltage of the e-beam was 20 kV in the e-beam lithography system. And the exposure dose was 160 $\mu\text{As}/\text{cm}^2$.
3. Metal deposition to form S/D contacts by e-beam evaporation. We deposited 30nm Au / 30nm Ag (contact layer) for Ag contacted MoS₂ FETs and 30nm Au / 30nm Ti for Ti contacted ones as the contact metals. The system pressure was kept at $\approx 1 \times 10^{-6}$ Torr during the metal deposition. The first 5nm of metal which directly contacted to MoS₂ was deposited at a lower rate of $\approx 0.2 \text{ \AA} / \text{sec}$ to improve the interface roughness, and rest of metal was deposited at a higher rate of $\approx 1 \text{ \AA} / \text{sec}$.
4. Lift off the metal by soak the sample into acetone over night at room temperature. The sample was rinsed with IPA and DI water after the acetone bath. The resulting devices have a channel length of 1 μm and contact width of 1 μm as well.

We also prepared samples for the interface characteristics. To do so much thinner metal film was e-beam evaporated on to exfoliated MoS₂. Samples for SEM, AFM and Raman spectroscopy are prepared in the same way except no e-beam lithography and lift off step and the thickness of metal deposited is thinner. 5nm Au / 5nm Ag and 5nm Au / 5nm Ti was deposited by e-beam evaporation. The top 5 nm Au is used as a capping layer

which protects the bottom contact layer from oxidizing. The e-beam evaporation conditions used are the same with device fabrication except that the deposition rate was kept at $\approx 0.2 \text{ \AA} / \text{sec}$ for the whole metal deposition process to mimic the device fabrication.

3.2.2 Characterizations:

The electric properties of MoS₂ FETs were tested in a vacuum probe-station. The system was kept at $\approx 1 \times 10^{-6}$ Torr during the measurement. A semiconductor parameter analyzer (HP 4156C) was used to carry out the electric measurement. The SEM is done with Zeiss Ultra-60 Field Emission SEM. An accelerate voltage of 5kV was used to capture the images. AFM images are taken with Dimension system controlled by Nanoscope V (Bruker, Santa Barbara, CA). All AFM experiments are performed with SCANASYST-AIR tip (Bruker, Santa Barbara, CA) with a radius of 10nm. AFM data are analyzed with WSxM software.[85] Raman spectra were acquired under ambient conditions with a micro-Raman spectrometer (Renishaw InVia Raman system) equipped with a 514.5nm (2.41 eV) wavelength excitation laser and an 1800 lines/mm grating while operating in 180° backscattering geometry. A 50X objective was used to focus the excitation laser to an approximately 1 μ m spot onto the sample. The 100% laser power is 4.8mW. We typically used 50% power to collect the signal for 1 second to compare the Raman spectra before and after metal deposition.

3.3 Results and Discussion

3.3.1 Electrical Characterization of MoS₂ transistors

Our devices were fabricated with exfoliated MoS₂ on 280 nm SiO₂/Si substrate. We deposited 30 nm Au/30 nm Ag for Ag contacted MoS₂ FETs and 30 nm Au/30 nm Ti for Ti contacted ones by e-beam evaporation. The resulting devices have a channel length of 1 μm and a contact width of 1 μm as well (**Figure 3.2(a)**).

Figure 3.2(b-d) shows the electric characteristics of monolayer MoS₂ transistors. We normalized the drain current (I_D) to the current density per 1 μm channel width (J_D) to compare the electrical characteristics of transistors with different channel width. Figure 3.2(b) compares the characteristics of J_D versus back gate voltage (V_{BG}) (J_D - V_{BG} characteristics) in monolayer MoS₂ transistors with Ag and Ti contacts. The devices were tested with V_{BG} varying from -100 V to 0 V and drain to source voltage (V_{DS}) equals to 50 mV or 1 V. All our devices show n-type MOSFET behaviours. The threshold voltage of the devices was extracted from the linear fitting of the ON-current versus V_{BG} with $V_{DS} = 50$ mV. The device threshold voltages are equal to -36.6 V and -45.4 V for Ag and Ti contacts, respectively. These results are reasonable since Ag and Ti have similar work functions. The devices with Ti contacts show a typical ON-current density, which is comparable to other back gated MoS₂ transistors without high-k dielectric passivation. [68-70] Most importantly, the devices with Ag contacts exhibit almost two orders of magnitude larger on-state current density than those with Ti contacts. We extracted subthreshold slope (SS) of the devices, which is given by:

$$SS = \left. \frac{dV_{BG}}{d(\lg(I_D))} \right|_{V_{DS}} \quad (1)$$

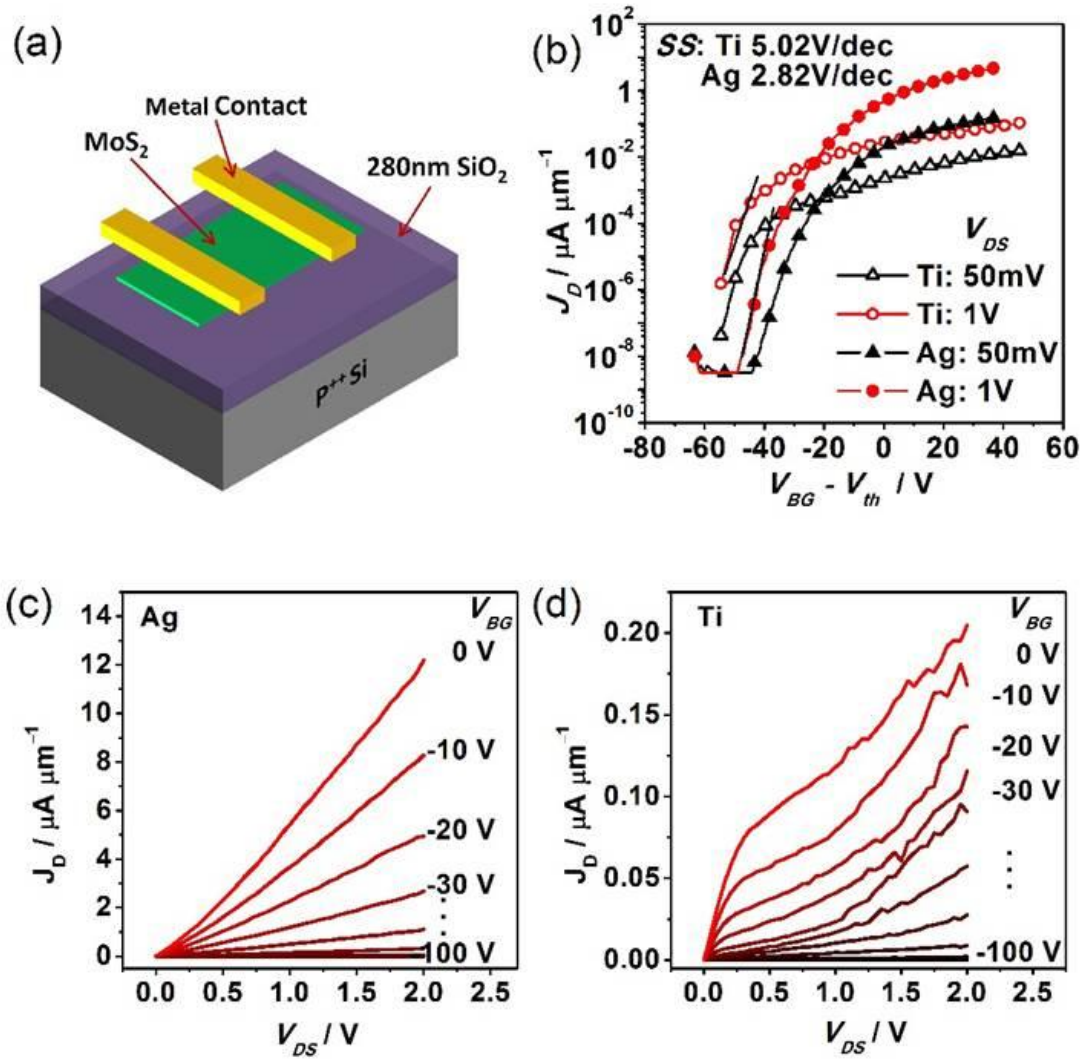


Figure 3. 2 MoS₂ transistor diagram and Drain current density of single-layer MoS₂ transistors: (a) MoS₂ transistor diagram Drain current density of single-layer MoS₂ transistors versus (b) $V_G - V_{th}$ with Ag or Ti contacts, and (c, d) drain voltage (V_{DS}) with (c) Ag or (d) Ti contacts.

SS was extracted from J_D - V_{BG} characterization at $V_{DS} = 1$ V. For devices with Ag contacts, the SS is 2.82 V/dec, and with Ti contacts, it is 5.02 V/dec. The large SS is partially due to the large thickness (280 nm) of back gate oxide. Similar SS value was also reported in the back-gated MoS₂ FETs in previous publications. [68, 70] The lower SS of devices with Ag contacts indicates the improved contact quality. It is clear that the device performance is significantly affected by the contacts. Better contacts bring about better electrostatics so that devices with Ag contacts show a lower subthreshold slope.

Figure 3.2(c) and (d) compare J_D - V_{DS} (source-drain voltage) characteristics of monolayer MoS₂ FETs with Ag and Ti contacts, respectively. The drain current was measured with V_{DS} varying from 0 to 2 V with V_{BG} varying from 0 to -100 V with a -10 V step. In Figure 3.2(c), the super-linear relationship between ON-state J_D and V_{DS} near zero in monolayer MoS₂ FETs with Ag contacts indicates the Schottky barrier transistor behaviour. In figure 3.2(d), the ON-state current density of MoS₂ FETs with Ti contacts is consistent with previous publications, [68, 70] and significantly smaller than the ones with Ag contacts. The linear dependence of J_D on V_{DS} could be a result of thermally assisted tunnelling, and may not necessarily indicate an Ohmic contact. [37] The current density of monolayer MoS₂ FET with Ag contacts is 60 times larger at $V_{BG} = 0$ V and $V_{DS} = 2$ V than that with Ti contacts. This larger magnitude of ON-current density reflects the higher carrier injection efficiency.

Figure 3.3 shows electrical properties of few-layer (2 to 3 layers) MoS₂ FETs. The drain current in these few-layer MoS₂ FETs was measured under the same bias conditions as the monolayer devices. In Figure 3.3(a), J_D - V_{BG} characteristics of few-layer

MoS₂ FET with Ag and Ti contacts were compared. All the devices show n-type MOSFET behaviour. The threshold voltage is -35.0 V for devices with Ag and Ti contacts. The subthreshold slope of transistors with Ag contacts is 5.42 V/dec. The devices with Ti contacts also show typical performance reported in previous publications. [68-70] The few-layer MoS₂ transistors with Ti contacts cannot be turned off completely even at V_{BG} = -100 V. Therefore, the subthreshold slope cannot be precisely extracted. Nonetheless, the comparison between these two devices does show improved current density and subthreshold slope with the Ag contacts.

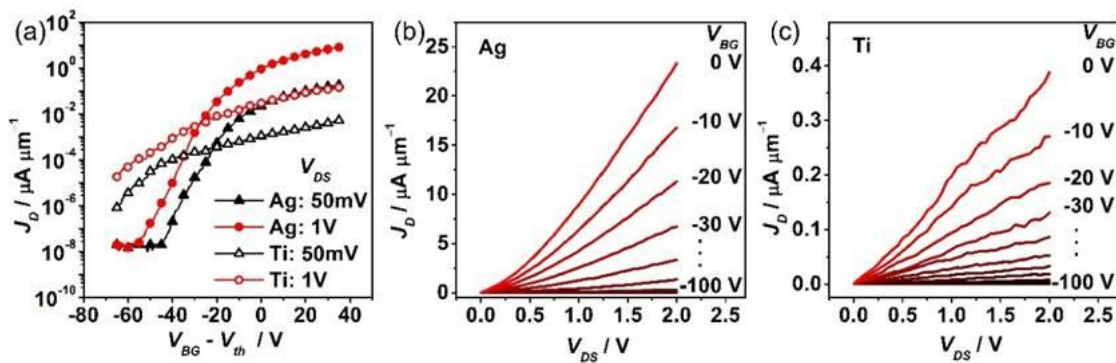


Figure 3.3 Drain current density of few-layer MoS₂ transistors versus (a) V_G-V_{th} with Ag or Ti contacts, and (b, c) drain voltage (V_D) with (b) Ag or (c) Ti contacts.

Figure 3.3(b) and (c) show J_D-V_{DS} characteristics of few-layer MoS₂ FETs with Ag and Ti contacts, respectively. Similar to monolayer MoS₂ FETs, a 60-time ON-state current enhancement is also shown in few-layer MoS₂ FETs with V_{BG} = 0 V and V_{DS} = 2 V.

As the contacting metal, Ag or Ti, is thick enough, the barrier height between MoS₂ and metal is dominated by the interaction between MoS₂ and the direct contact metal layer. Here, Ag and Ti have very similar work functions (4.26 eV for Ag and 4.33 eV for Ti). [72] Interestingly, theoretical simulations have shown that Ti is a better contact with WSe₂ than Ag, [66, 71] experimental results show that the devices with Ag contacts perform much better than those with Ti. [66] To gain a better understanding, we performed the surface and interface characterization on our metal contacts.

3.3.2 Surface Morphology of Metal Thin Films on MoS₂

To understand the performance difference, we deposited 5 nm Ag or 5 nm Ti on top of exfoliated MoS₂ followed by the deposition of 5 nm Au as protection layer. The conditions used are the same with device fabrication except that the deposition rate was kept at $\approx 0.2 \text{ \AA}/\text{sec}$ for the whole metal deposition process to mimic the device fabrication.

Then, SEM was carried out to characterize their surface morphology. From SEM images (**Figure 3.4**), the morphology of Au/Ag or Au/Ti films on MoS₂ is found to be significantly different. Figure 3.3(a) shows that the Au/Ag morphology on MoS₂ and on SiO₂/Si substrate is so distinct that MoS₂ area can be clearly identified. Au/Ag forms surprisingly a much smoother and denser film on MoS₂ than on SiO₂/Si. In contrast, with the appearance of pinholes, Au/Ti film shows quite similar morphology on both MoS₂ and SiO₂/Si (Figure 3.4(b)). Therefore, the location of monolayer MoS₂ is very difficult to identify, though we can still identify it through its edges.

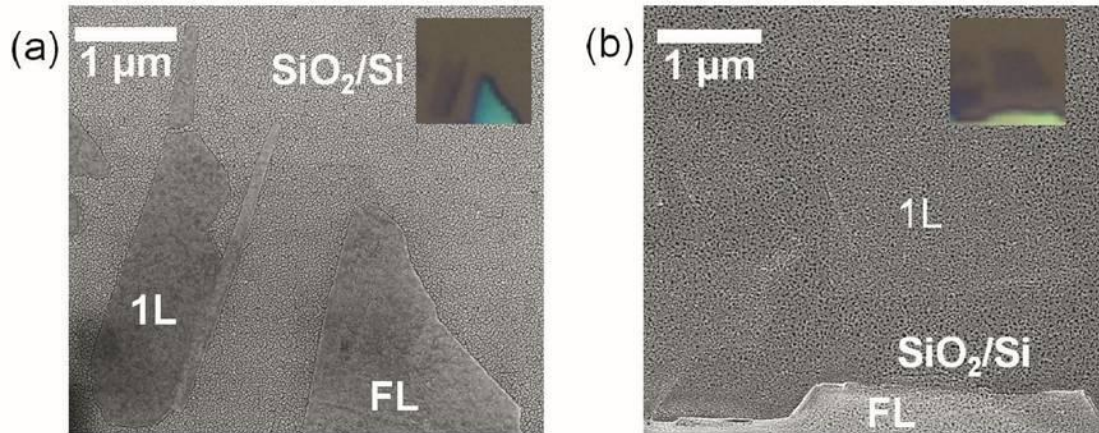


Figure 3.4 SEM images of MoS₂ on SiO₂/Si substrate after (a) Au / Ag deposition and (b) Au/Ti deposition. The insets show corresponding optical image of pristine MoS₂ before metal deposition. The locations of monolayer MoS₂ (1L) and few-layer MoS₂ (FL) are identified after metal deposition.

AFM was used to further analyze the surface roughness of the metal films. As seen in the AFM images (**Figure 3.5**), topography of the metals on MoS₂ and SiO₂/Si substrate exhibits significant difference. Au/Ag on MoS₂ is smoother than on SiO₂/Si (Figure 3.5(a)). A line profile shows that the surface of Au/Ag on monolayer MoS₂ is 0.54 nm lower than on SiO₂/Si on average (Figure 3.5(b)). Since the same amount of metal is deposited on the surface, a smoother and denser metal film (Au/Ag) on MoS₂ results in a thinner film than that on SiO₂/Si, even with the additional layer of MoS₂ underneath. The normalized height histograms of Au/Ag also show a narrower height distribution on MoS₂ than on SiO₂/Si (Figure 3.5(c)). The root mean squared (RMS) surface roughness is 0.37 nm on MoS₂, but 0.61 nm on SiO₂/Si. For Au/Ti, however,

pinholes are clearly seen on both MoS₂ and SiO₂/Si (Figure 3.5(d)). The surface of Au/Ti on MoS₂ is 2.18 nm higher than that on SiO₂/Si (Figure 3.5(e)). This is reasonable by considering the height of MoS₂ and its interfaces. The metal surface roughness is almost the same on MoS₂ and on SiO₂/Si (Figure 3.5(f)): RMS roughness is 1.08 nm and 1.09 nm on MoS₂ and on SiO₂/Si, respectively. Clearly, the Au/Ag film is much smoother than the Au/Ti film on MoS₂.

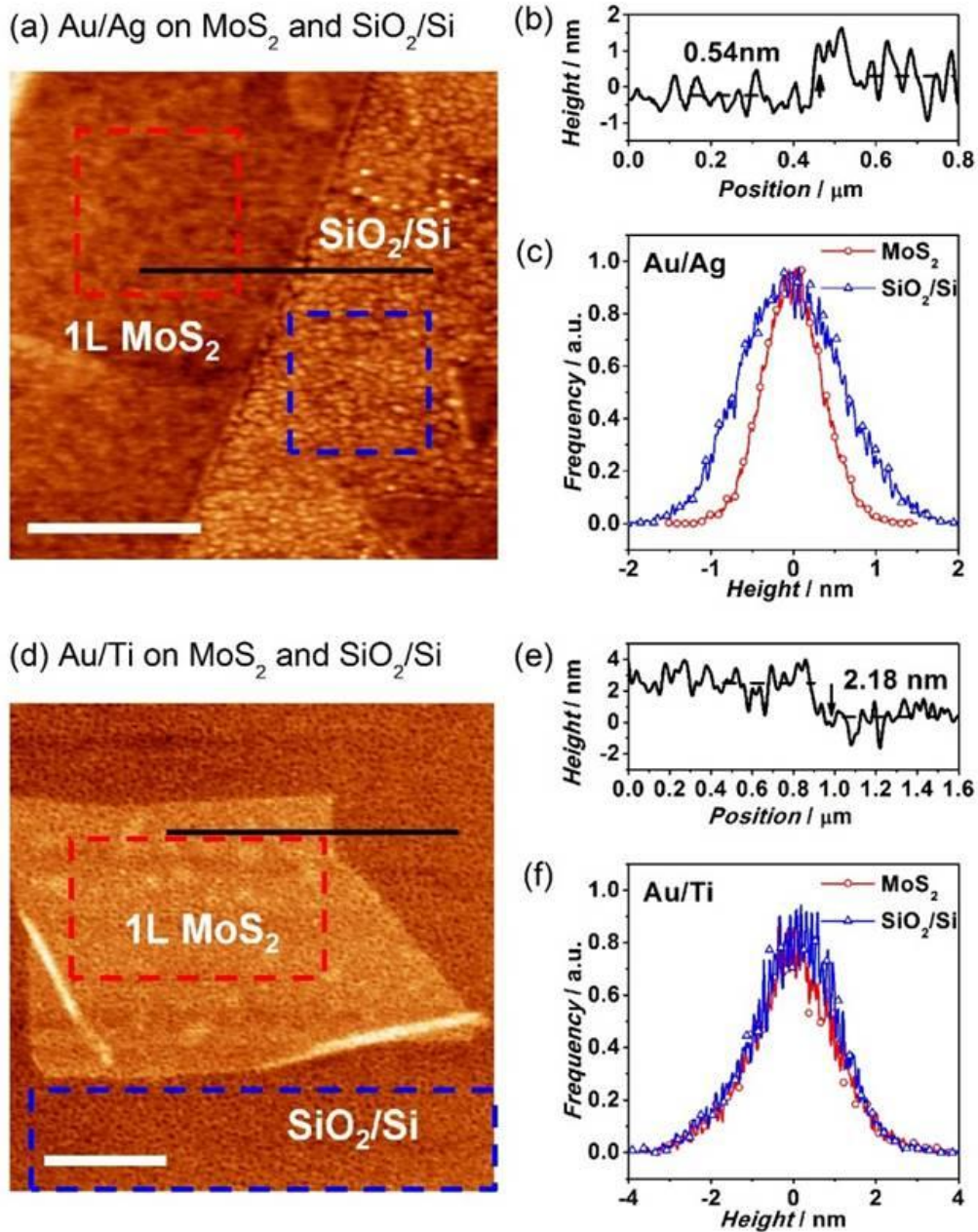


Figure 3.5 AFM and roughness analysis of metal on MoS₂ and SiO₂/Si substrate: (a) Topography of Au/Ag on MoS₂ and SiO₂/Si. (b) A topographic line profile of the height along the slide line indicated in figure (a). (c) Normalized histograms of height distribution of areas indicated by the square in figure (a). (d) Topography of Au/Ti on MoS₂ and SiO₂/Si. (e) A topographic line profile of the height along the slide line indicated in figure (d). (f) Normalized histograms of height distribution of areas indicated by the square in figure (c). Scale bars are 500 nm long for image (a) and (d).

3.3.3 Raman Spectroscopy of MoS₂ Covered with Metal

Recently, Raman spectroscopy has been used to investigate the effects of metal-MoS₂ interface on the electronic and phonon properties of MoS₂. [86] We carried out our Raman spectroscopy measurements on mono- and few-layer MoS₂ before and after deposition of the thin metal films (5 nm Au/5 nm Ag or 5 nm Au/5 nm Ti).

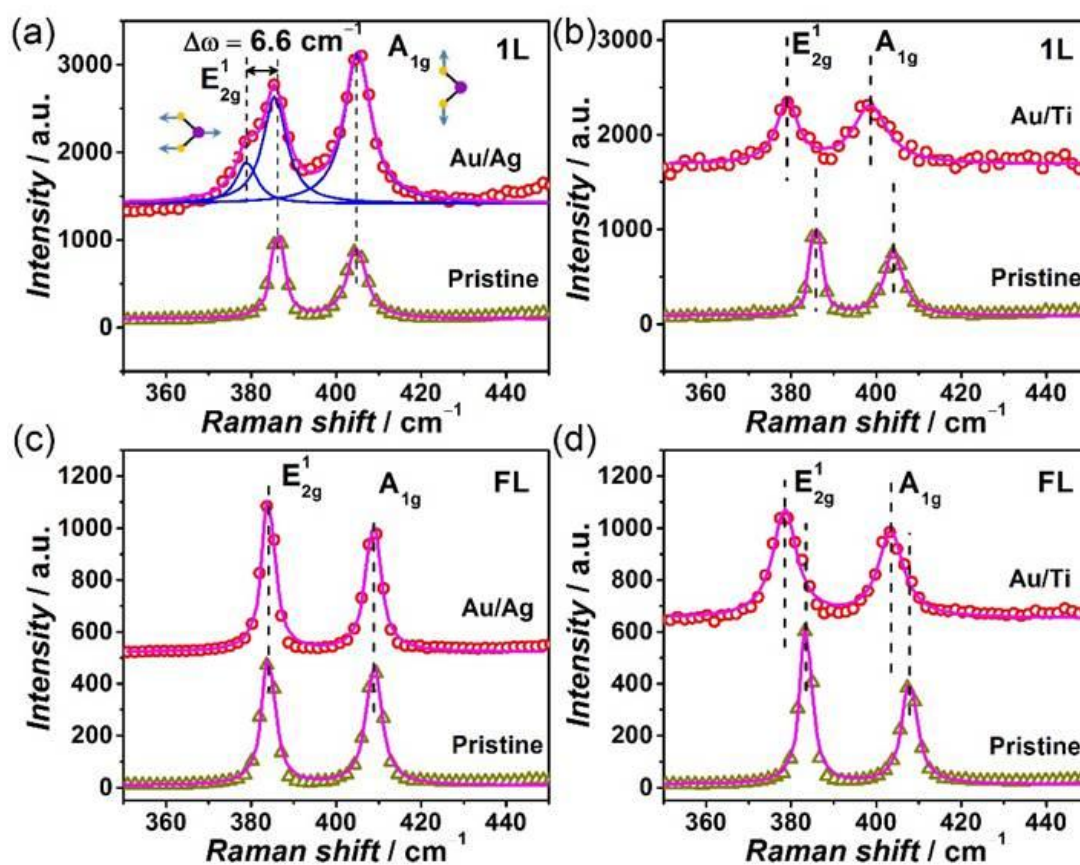


Figure 3.6 Comparison of Raman spectra before and after (a) Au/Ag or (b) Au/Ti deposition on monolayer (1L) MoS₂ and before and after (c) Au/Ag or (d) Au/Ti deposition on few-layer (FL) MoS₂. The scatters are real data and solid lines are fitted Lorentz peaks.

Figure 3.6 shows the representative Raman spectra of MoS₂ before and after metal deposition. Before metal deposition, the Raman spectrum of the pristine MoS₂ shows E_{2g}^1 mode and A_{1g} mode peaks (Figure 3.6(a)). The E_{2g}^1 mode is the in-plane MoS₂ lattice vibration mode where the two sulfur layers move in the same direction collectively parallel to the lattice plane while the Mo moves in the opposite direction. These two peaks are symmetric and each is fitted well with a single Lorentz peak. And the A_{1g} mode represents the out-of-plane lattice vibration with the sulfur atoms on both sides of Mo atoms moving in the opposite directions vertical to the lattice plane while keeping Mo atoms in place. For pristine monolayer MoS₂, the Raman shift difference between these two peaks is 18.6 cm⁻¹ for the Au/Ag sample and 18.3 cm⁻¹ for the Au/Ti sample (Figure 3.6(a) and (b)). After Au/Ag deposition, there is no significant change in peak position for A_{1g} mode (Figure 3.6(a)). However, the E_{2g}^1 mode of MoS₂ splits into two peaks with a separation of 6.6 cm⁻¹. Also the higher frequency peak of E_{2g}^1 mode red shifts by 0.7 cm⁻¹ compared to pristine monolayer MoS₂. The more significant effects of Au/Ag deposition on E_{2g}^1 mode indicate that the metal deposition affects the in-plane lattice vibration more than the out-of-plane. C. Gong *et al.* compared Raman spectra of monolayer MoS₂ with different metal depositions,[86] and their results show stronger effects on E_{2g}^1 mode than on A_{1g} mode by Au and Ag deposition. In Ag covered monolayer MoS₂, E_{2g}^1 peak splits into two peaks. The peak at higher frequency remains in the same position with the E_{2g}^1 peak of pristine MoS₂ and the other red-shifts by 6.38 cm⁻¹. [86] But, in their Au covered monolayer MoS₂, the E_{2g}^1 peak is broadened and red-

shifts with only 3.8 cm^{-1} peak split. [86] In our Au/Ag covered monolayer MoS₂, the E_{2g}^1 peak split is 6.6 cm^{-1} and the peak at high frequency red-shifts very little compared to the pristine monolayer MoS₂. This peak splitting is very similar to the Ag covered monolayer MoS₂ sample observed by C. Gong *et al.* [86] It indicates that in our sample, Au does not penetrate through Ag to make a direct contact with MoS₂ and Ag is indeed the contact metal.

After the deposition of Au/Ti film on monolayer MoS₂, both E_{2g}^1 and A_{1g} peaks red-shift and are broadened significantly (Figure 3.6(b)). However, each peak still remains symmetric and can be fitted with a single Lorentz peak. Even though there are pinholes in Au/Ti film on MoS₂, on the basis of the work by C. Gong *et al.*, [86] the absence of E_{2g}^1 peak splitting indicates that the contacting layer is Ti instead of Au.

We can now explain the dramatic topographic difference between Au/Ag and Au/Ti films on MoS₂. It is reasonable to correlate this difference with the roughness of the contact layer. Raman spectroscopy reveals that the contact layer with MoS₂ is Ag and Ti for Au/Ag and Au/Ti films, respectively. As a result, the smoother topography observed with the Au/Ag film indicates the smoother Ag contacting layer with MoS₂. Ag has exhibited a good wettability on bulk MoS₂. [67] Our results show that this good wettability is preserved on mono- and few-layer MoS₂ as well.

As we did not anneal our devices for the electrical measurements, the performance difference cannot be simply attributed to the chemical react between Ag and MoS₂ because previous work has shown that Ag does not react with MoS₂ at room

temperature. [87] Therefore, it is reasonable to believe that the MoS₂ FET performance is enhanced by the better contacting interface between Ag and MoS₂.

For the Au/Ag covered monolayer MoS₂, the in-plane E_{2g}^1 mode splits while the out-of-plane A_{1g} mode keeps its place. This change in Raman spectra after metal deposition is unlikely due to some vertical perturbations such as the pressure introduced by top metal and chemical bonds formed with metal atoms deposited on top. These vertical perturbations would affect out-of-plane A_{1g} mode more than E_{2g}^1 mode which is not complied with our results. The E_{2g}^1 peak splitting should be the result of the in-plane strain introduced by metal deposition. Previous studies [86, 88, 89] demonstrated the influence of uniaxial tensile strain on MoS₂ phonon modes. Their results showed that the out-of-plane A_{1g} mode was not shifted by strain while the in-plane E_{2g}^1 mode was split 4.5 cm⁻¹ by 1% strain. Therefore, we estimate that the Au/Ag film introduces 1.46% strain into our MoS₂ sample ($6.6 \text{ cm}^{-1} \div (4.5 \text{ cm}^{-1}/1\%) = 1.46\%$). In contrast to monolayer MoS₂, few-layer MoS₂ did not show such significant changes in the Raman spectrum after Au/Ag deposition (Figure 3.6(c)) and both peaks stay at almost same positions. A. Castellanos-Gomez *et al.* studied the localized uniaxial strain influences on the few-layer MoS₂ Raman spectra. [90] They found that in few-layer (3~5 layers) MoS₂, both E_{2g}^1 and A_{1g} modes red-shift with strain, whereas E_{2g}^1 mode shifts larger, about 1.7 cm⁻¹ per 1% strain. The absence of the peak shift in our Au/Ag covered few-layer MoS₂ indicates that the tensile strain introduced by metal deposition might be thickness dependent.

On the monolayer MoS₂ after Au/Ti deposition, the E_{2g}^1 peak red-shifts by 6.7 cm⁻¹, and A_{1g} by 5.5 cm⁻¹ (Figure 3.6(b)). The simultaneous peak shifts of E_{2g}^1 and A_{1g} modes clearly indicate the temperature increase in the samples during the Raman measurement. The Raman modes of monolayer MoS₂ affected by temperature have been investigated in the literature: Both E_{2g}^1 and A_{1g} peaks red-shift when temperature increases. [91-95] From the red-shifts of the both peaks in our samples, the temperature of Ag/Ti covered monolayer MoS₂ increased significantly during the Raman measurement. This heating effect was also observed in the Raman spectrum of few-layer MoS₂: the two peaks also red-shift simultaneously after Au/Ti film deposition (Figure 3.6(d)). The peak red-shifts are 5.0 cm⁻¹ for E_{2g}^1 mode and 4.2 cm⁻¹ for A_{1g} mode.

The temperature increase in Au/Ti coated MoS₂ is due to the laser heating during Raman measurement. To confirm this, we performed Raman measurements with different power and signal collection time on monolayer MoS₂ covered by thin layer Au/Ti (**Figure 3.7**). When the power is as low as 10% of the total laser power, and the signal collection time is 10 seconds, no significant peak shift was observed. However, as the laser power increases or signal collection time gets longer, the peak shift becomes more significant. This indicates that the peak shift is a result of the laser heating of the sample.

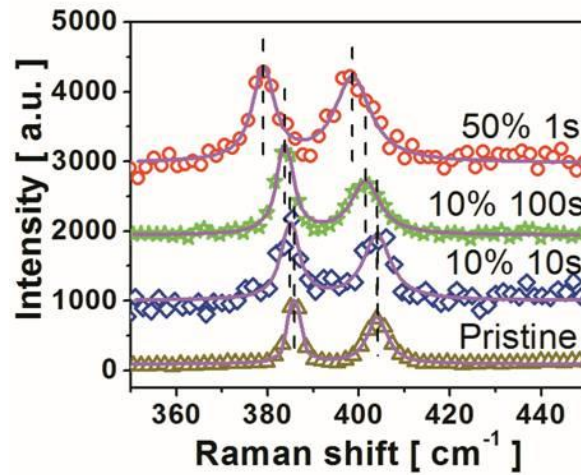


Figure 3. 7 Raman spectra on Au/Ti covered MoS₂ with different power and signal collection time. Scatters are experimental data and solid lines are fitted curves.

It is interesting to see that the heating effect is not seen in pristine and Au/Ag covered MoS₂. The dramatic difference of thermal conductivity between Ag and Ti could contribute to the difference in heating effect between Au/Ag covered MoS₂ samples and Au/Ti covered ones. At room temperature, the thermal conductivity of Ag is almost 20 times larger than Ti. [96] The higher thermal conductivity of Ag and the smoother and denser morphology of the Ag film enhance the heat dissipation efficiency. Therefore, the heating effect is weaker in Au/Ag covered MoS₂ samples. We also notice that the heating effect occurs on mono- and few-layer MoS₂ covered with Au/Ti. On the thicker MoS₂, the heating effect is not significant. This phenomena probably is related to the strong photoluminescence from mono- and few-layer MoS₂ and its interaction with Ti under ambient conditions.

3.4 Conclusion

In summary, both monolayer and few-layer MoS₂ FETs with Ag source/drain contacts show 60-time larger on-state current and a steeper subthreshold slope than those with Ti contacts. SEM and AFM both show that the topography of Au/Ag film on MoS₂ is significantly smoother and denser than Au/Ti film. Raman spectroscopy revealed that the contact layers are Ag and Ti in these two cases. It is reasonable to conclude that the smoother and denser Ag contact leads to higher carrier transport efficiency, and is the main reason for the performance enhancement. Also, the high thermal conductivity can be a benefit for the heat dissipation during device operation. Considering that proper source/drain metal contacts are crucial for forming higher quality MoS₂ transistors, our result indicates that the metal/MoS₂ interface morphology is a crucial parameter to consider when optimizing electrical contacts.

CHAPTER 4: GATE EFFECTS AND CURRENT CROWDING IN METAL/MoS₂ CONTACTS

4.1 Introduction

Recently, mono- and multi-layer MoS₂ have attracted a lot of attention for future electronic and photonic applications. [10, 11] MoS₂ is a 2-dimensional (2D) semiconductor which has a bandgap ranging from 1.2 eV to 1.8 eV depending on its thickness. [14, 15, 27] In particular, monolayer MoS₂ with a direct bandgap of 1.8 eV shows promising electric and optoelectronic applications. [9, 50-54] In addition, considering short channel effects in metal-oxide-semiconductor field effect transistors (MOSFETs), the intrinsic ultrathin body of mono-layer MoS₂ also represents the ultimate in scaling. [56] The intrinsic ultrathin body and robust lattice structure in 2D MoS₂ are also attractive for flexible electronic applications.[19, 20, 55]

However, MoS₂ transistor performance remains a bottleneck for MoS₂ future applications. To improve MoS₂ transistor performance, the Source/Drain (S/D) contacts are very important factors to consider. A variety of contacts have been used and studied to achieve a good Ohmic contact on MoS₂. [37, 38, 55, 62-64, 71, 97] At beginning the research is focused more on the mechanism at the barrier in metal-MoS₂ interface. [37, 38, 62, 71, 97] Fermi level pinning in metal contacts makes the MoS₂ FETs mainly n-type. [37, 38] And the intrinsic defects in MoS₂ leads to significant variation in contact

behaviour even when same metal contacts are used. [62] Later the current distribution under the metal contacts is also considered. [70, 73] However, their results are based on back-gate devices where the channel current was not well tuned by the gate. Moreover, in bottom-gate MoS₂ transistors, the Fermi level of MoS₂ under the contacts is not screened from the gate bias by the metal which is not the case in top-gate transistors. Our previous work shows that gate-assisted test structure is a good approach to test the contacts in low-dimensional electric system. [74] In this article, we present our work on the current crowding effect in metal-MoS₂ contacts which is affected significantly by a top gate.

We fabricated Ag contacted bilayer MoS₂ transistors with 30 nm Al₂O₃ top gate on 300 nm SiO₂/Si substrate. The dimensions of our transistors are: 0.5 μm channel length, 4 μm channel width and 1 μm contact length. Ag was chosen because it has been reported to form a good contact on WSe₂, [66] which is a similar material to MoS₂. And our previous work shows Ag forms smooth and solid film on MoS₂ which makes the carrier transport efficiently across the contacts. Our devices show good n-type current-voltage (I-V) characteristics. Then gate assisted Kelvin structure and 4-probe method was used to analyze the contacts. The contact resistance extracted from the both methods is significantly different due to the difference in position where the voltage is sampled in both methods. By comparing the contact resistance extracted from both methods, we find the current transfer length (L_T) of Ag-contact MoS₂ transistors is 137 nm to 206 nm which increased with the increase of gate voltage. The channel sheet resistance is also measured by 4-probe method. It is much larger than the contact resistance which indicates that the MoS₂ transistors are channel-dominant. The contact resistivity is also

extracted from our data. It is effectively tuned by the gate as well. Our result shows that considering the contact resistance, the gate affects not only the contact resistivity but also the current crowding in the contacts.

4.2 Growth of MoS₂ and Device Fabrication

Our MoS₂ transistors were fabricated with chemical vapour deposited (CVD) MoS₂ on 285nm SiO₂/Si substrate. The CVD was performed with MoO₃ and sulfur as the precursor. About 5 mg MoO₃ was placed in an alumina crucible in the center a tube furnace. Then abundant amount (1~2 g) of sulphur in alumina crucible was allocated at the entrance of the furnace. And the 285 nm SiO₂/Si substrate was place 2 cm downstream to MoO₃. The furnace set-up was illustrated in Fig. 4.1(a). 100 sccm Ar was used as carrier gas and the pressure was kept at 800 Torr during the CVD. Before the heating process, the whole system was pumped to 200 mTorr and then flushed with Ar to achieve the set-up pressure. The pump-down and flush process was repeated 3 times and a stable pressure of 800 Torr was achieved before the heating process started. The heating process includes 30 minutes ramping up to 850 °C and a hold at 850 °C for 30 minutes. After heating, the tube furnace was naturally cooled down to below 200 °C before the samples were replaced from the furnace.

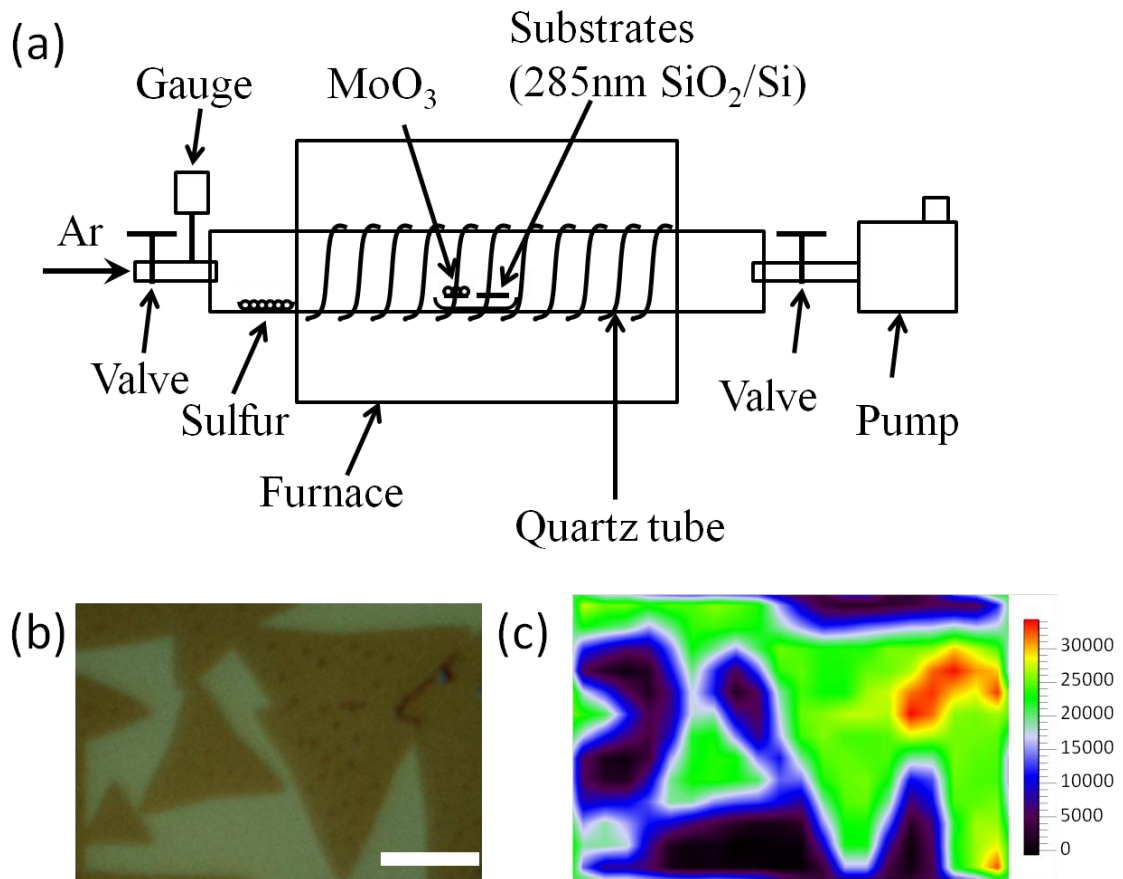


Figure 4. 1 (a) System set-up for MoS₂ CVD. (b) Image of typical MoS₂ flakes grown on SiO₂/Si substrate. The scale bar is 5 μ m. (c) Device schematic.

The resulting samples are MoS₂ flakes spreading over the 285 nm SiO₂/Si substrate. The MoS₂ flakes are typically triangular or hexagonal shaped. (Fig. 4.1(b)) The Raman mapping of the intensity of two representative peaks shown in Fig. 1(c) indicates the MoS₂ flake thickness is uniform. The Raman spectra of a representative point on the MoS₂ flakes shows the distance between the two major peaks is 21 cm⁻¹, indicating they are 2 layers in thickness. For the contact measurement, only Ag contacts are used. As discussed in Chapter 3, Ag is a much better material to form S/D contacts.

The MoS₂ flakes were allocated with a microscope and then conventional lithography process was used to define the devices. 50 nm Au/ 5nm Ag was used as the source/drain (S/D) contacts. 5 S/D contacts were parallel placed on a same triangle flake of MoS₂ so that contact test can be carried with these contacts later. The channel length of the transistors is 0.5 μm and the contact length is 1 μm. Then the rectangular channel was defined by O₂ plasma etching. 1 nm Al was deposited and then oxidized in air as seeding layer for atomic deposition (ALD) of 30 nm Al₂O₃ to promote the gate dielectric quality.[98] Al₂O₃ ALD was performed at 300 C with trimethylaluminum (TMA) and H₂O as precursor. Finally, 50 nm Au / 5 nm Ti was used as top gate electrode. The top gate covers the whole region where the 5 S/D contacts are placed so that the channels are common gated. The resulting device structure is illustrate in Fig. 4.2(a). Fig. 4.2(b) shows the scanning electron microscopic image of two adjacent channel with three contacts. The channel length and contact length are measured to be 370 nm and 1.09 μm respectively.

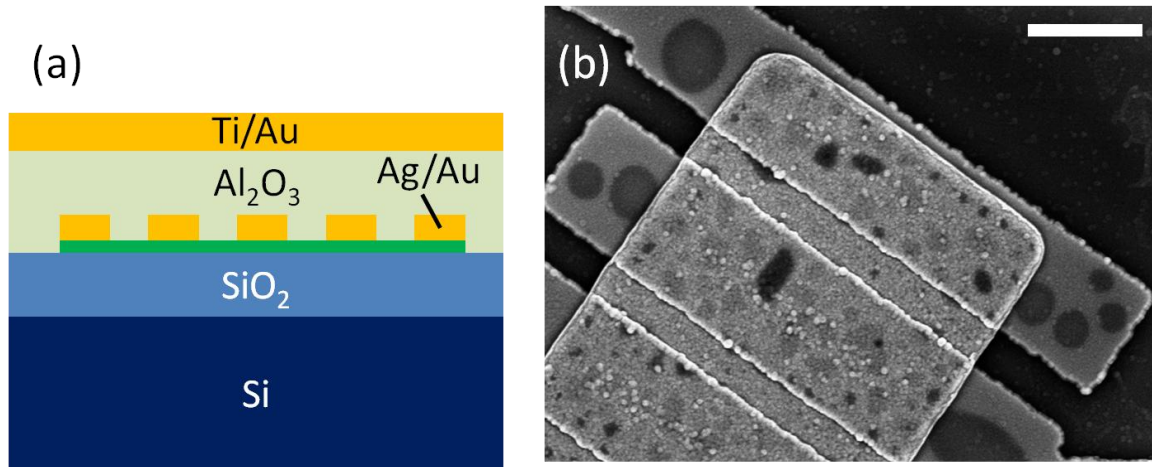


Figure 4.2 Device structure: (a) Schematics of MoS₂ FETs (b) SEM image of a MoS₂ transistor. Scale bar in this image is 1 μm .

4.3 Results and Discussion

The devices were then tested with a semiconductor parameter analyser (Hewlett-Packard® 4156) in a probe station (Cascade® summit semi-automated probe station) at room temperature.

The I-V characterization of a typical MoS₂ with 30 nm Al₂O₃ gate dielectric was shown in Fig. 2. The channel current is normalized to the current per 1 μm channel width. From Fig. 4.3(a), the transistor shows a strong n-type behaviour which is consistent with previous papers.[19, 37, 50, 55] In Fig. 4.3(b), the ON-current of our device is quite high compared to the devices in previous demonstrations. And the linear relationship between drain current (I_D) and applied drain voltage (V_D) at low voltage voltage indicates good S/D contacts for the transistors.

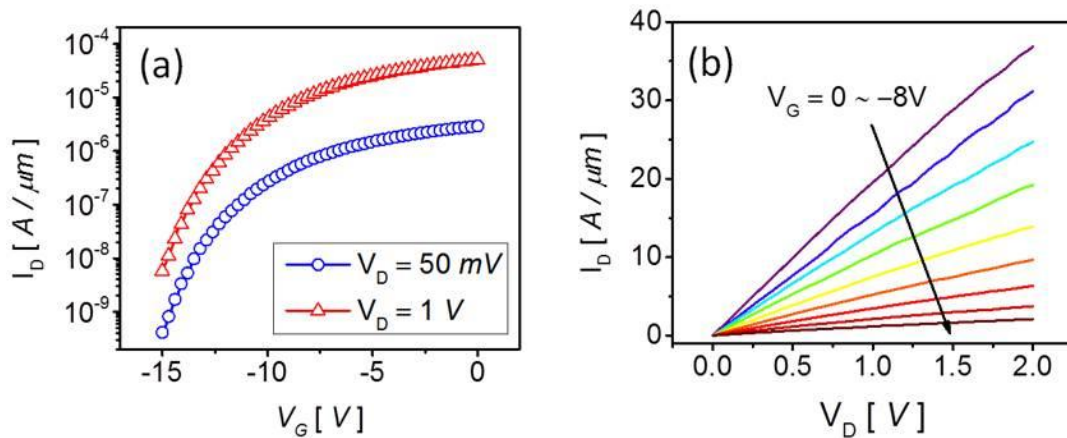


Figure 4.3 I-V characterization of a representative MoS₂ FET: (a) I_D - V_G , and (b) I_D - V_D characteristic.

To evaluate the metal contacts on MoS₂, gated assisted Kelvin test and 4-probe test were done on the MoS₂ transistors. Fig. 4.4 shows the result of the gate assisted Kelvin test. The measurement set-up is illustrated in the inset of Fig. 4.4(a). In Kelvin test structure, the current (I_D) is driven by a current source which is applied between source and drain contact, and the non-locate voltage (V_{23}) was read from the grounded source contact and an extra electrode which is connect to MoS₂ across another channel. Since a common gate is applied to our transistors, the both channel should be conducting simultaneously. As no current flows through the extra contact, the voltage on it should be equal to the voltage on MoS₂ at the end of source contact. So V_{23} is the voltage drop on the end of MoS₂ under the contact on source electrode. V_{23} versus I_D at different gate voltage is shown in Fig. 4.4(a). The linear relationship between V_{23} and I_D indicates an Ohmic contact. The overlap of the V_{23} curve at different V_G shows the contact resistance extracted by Kelvin test method (R_{C-K}) is not strongly affected by V_G . Figure 4.4(b) shows

the R_{C-K} which is extracted from the linear fitting of V_{23} on I_D . The value of R_{C-K} is slightly larger than 20Ω , which is much lower than the contact resistance extracted from other methods in previous publications. [70, 73, 97]

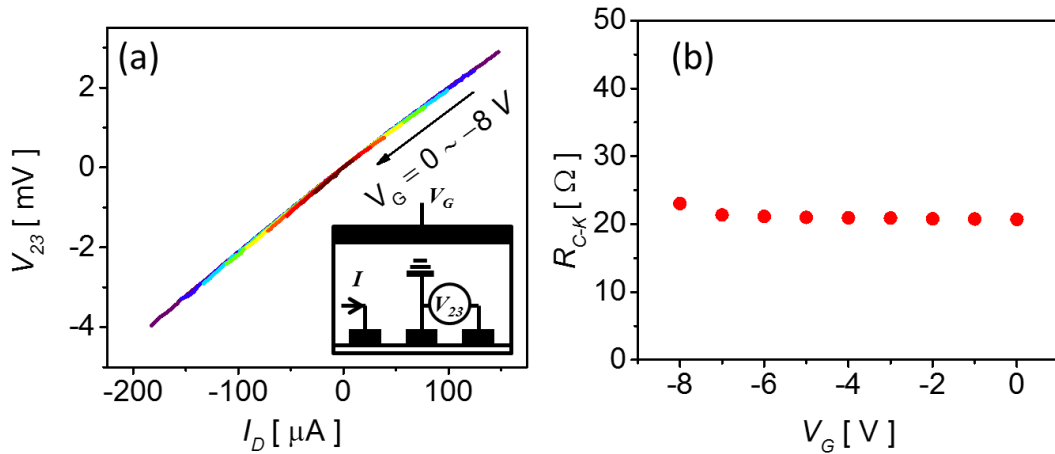


Figure 4.4 Gate assisted Kelvin test: (a) V_{23} - I_D measured at different V_G , inset is the illustration of the measurement set-up; (b) R_{C-K} extracted from the linear fitting of V_{23} and I_D at different V_G .

Then a 4-probe measurement was done to extract the contact resistance and further understand the contact behaviour. The measurement set-up is shown in inset of Fig. 4.5(a). A voltage source was connected to the S/D contacts at the ends to drive the current through the channel under the gate voltage varying from -5 V to 0 V. The I_D and the voltage difference between two middle contacts is measured at the same time so that the channel sheet resistance can be extracted by the linear fitting of voltage drop between two middle contacts and I_D in linear region. The contact resistance (R_C) can be evaluated

by subtracting the channel resistance (R_{ch}) from the total resistance (R_{tot}), which can be expressed as:

$$R_c = \frac{1}{2}(R_{tot} - R_{ch}). \quad (4.1)$$

Here, the channel resistance is estimated from the channel sheet resistance.

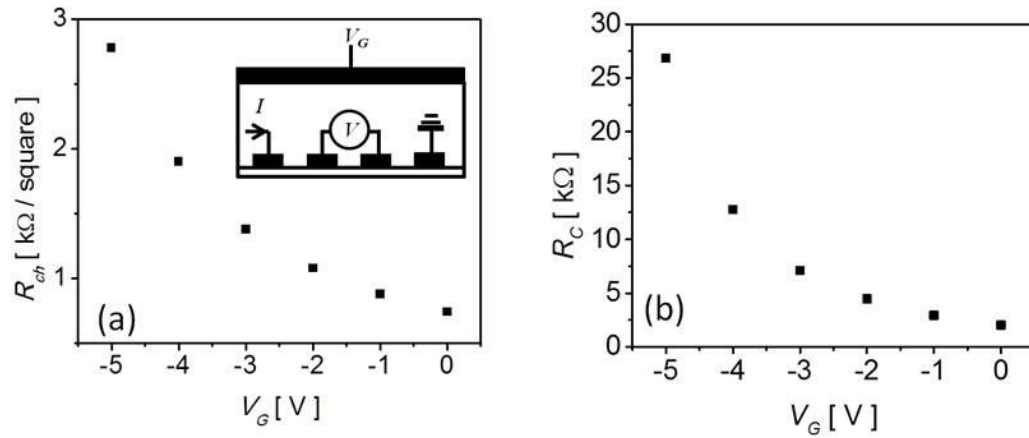


Figure 4.5 Gate assisted 4-probe measurement. (a) Channel sheet resistance at different V_G , inset is the measurement set-up for gate assisted 4-probe measurement. (b) Contact resistance (R_c) extracted from 4-probe measurement.

Fig. 4.5 shows that both the channel sheet resistance and contact resistance changes with gate voltage. As shown in Fig. 4.5(a), the channel conductance is effectively tuned by the gate, which is expected. As shown in Fig 4.5(b), it is interesting that the contact resistance is also affected by the gate. Compared to channel resistance, the contact resistance is much lower in our transistors. This indicates that the channel properties dominate our MoS₂ transistor performance.

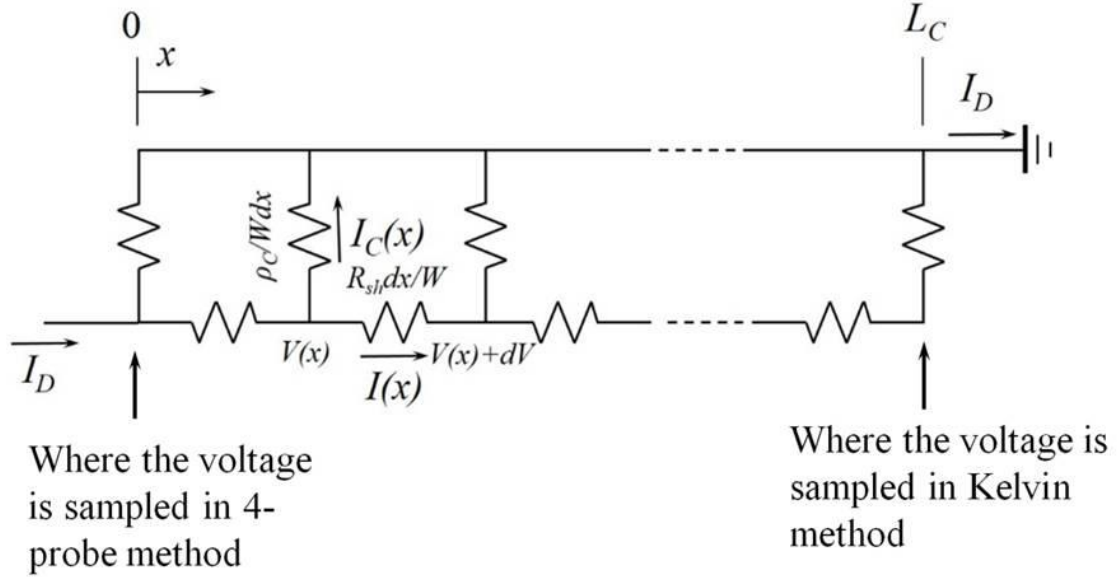


Figure 4.6 TLM model for contact resistance. The positions where the voltage is sampled in Kelvin method and 4-probe measurement are pointed.

Furthermore, compared to R_{C-K} , R_C is much larger and changes with the gate voltage. This difference is due to the difference in position where the voltage is sampled in these two contact characterization method. According to transmission line model (TLM, illustrated in Fig. 4.6), the current ($I(x)$) and voltage ($V(x)$) at position x have the relation as: [46, 75, 79, 99]

$$-dI(x) = I_C(x) = \frac{WV(x)dx}{\rho_C} \quad (4.2)$$

$$\frac{R_{sh}dx}{W} I(x) = -dV(x) \quad (4.3)$$

where R_{sh} is the sheet resistance of the semiconductor under the contact, and $I_C(x)$ is the current transport from the semiconductor to the contact at position x , W is the contact width, and L_C is the contact length.

Substitute eq. (4.2) into Eq. (4.3), we get,

$$\frac{\rho_C}{R_{sh}} d^2 I(x)/dx^2 = I(x) \quad (4.4)$$

Let $L_T = \sqrt{\rho_C/R_{sh}}$, L_T is the current transfer length in the contact, then we can solve Eq. (4.4), and get,

$$I(x) = Ae^{x/L_T} + Be^{-x/L_T} \quad (4.5)$$

At the boundaries of $x = 0$ and $x = L_C$, we have the current $I(0)$ and $I(L_C)$ which are:

$$I(0) = I_D \quad (4.6)$$

$$I(L_C) = 0 \quad (4.7)$$

So the expression for current at position x is,

$$I(x) = I_D \frac{\sinh [(L_C-x)/L_T]}{\sinh (L_C/L_T)} \quad (4.8)$$

Then we can get the voltage at position x as,

$$V(x) = -\frac{\rho_C}{W} \frac{dI(x)}{dx} = \frac{\sqrt{\rho_C R_{sh}} \cosh ((L_C-x)/L_T)}{W \sinh (L_C/L_T)} I_D \quad (4.9)$$

In Kelvin test structure, the voltage on the contact is sampled at the end of the contact, so,

$$R_{C-K} = \frac{V(L_C)}{I_D} = \frac{\sqrt{\rho_C R_{sh}}}{W \sinh(L_C/L_T)}. \quad (4.10)$$

However, in 4-probe method, the voltage on the contact is sampled in the front of the contact, so,

$$R_C = \frac{V(0)}{I_D} = \frac{\sqrt{\rho_C R_{sh}} \cosh(L_C/L_T)}{W \sinh(L_C/L_T)}, \quad (4.11)$$

It is clear that the ratio of R_C to R_{C-K} can be expressed as:

$$\frac{R_C}{R_{C-K}} = \cosh(L_C/L_T). \quad (4.12)$$

So, compare the contact resistance we got from both methods, we can extract L_T in our devices. The result is shown in Fig. 4.7(a). It is clear that the transfer length is also affected by the gate voltage. The value increases from 138 nm when V_G equals to -5 V to 206 nm when V_G equals to 0 V. These values are consistent with the previous work. [73] It is clear that the L_C is much longer than L_T in our devices. The voltage drops as long as the current is concentrated at the front part of the contact. The R_C can be approximately expressed as:

$$R_C \approx \frac{\sqrt{\rho_C R_{sh}}}{W} = \frac{\rho_C}{WL_T}. \quad (4.13)$$

So the contact resistivity ρ_C can be extracted. As shown in Fig. 4.7(b), it decreased with the increase of gate voltage. As the contact resistivity is concerned with the barrier between MoS₂ and the metal, the gate voltage also modulate the barrier at the contact.

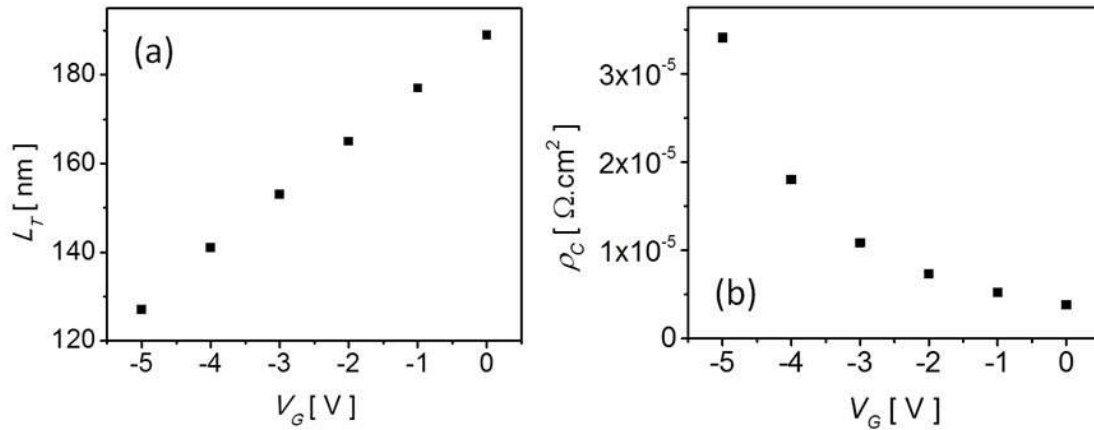


Figure 4.7 (a) Current transfer length and (b) Contact resistivity at different V_G .

In general, the gate has strong effects on contact resistance of MoS₂ transistors. The transfer length increases and contact resistivity decreases when gate voltage increases, so that the contact resistance decreases as a result.

4.4 Conclusion

In summary, n-type MoS₂ FETs were fabricated with a conventional lithography process. All MoS₂ transistors show good I-V characterizations. The contacts of the MoS₂ transistors were then analyzed with gate assisted contact measurement including Kelvin structure and 4-probe methods. The contact resistance extracted from these two methods is significantly different. According to TLM model, this difference is due to the current crowding and the difference in positions where the voltage is sampled in both methods. The current transfer length is extracted based on the ratio of the contact resistance extracted from these two methods. Transfer length increases with the increase of the gate

voltage. Channel resistance which is measured by the 4-probe method is much larger than the contact resistance. It indicates that our MoS₂ transistors are channel dominant devices. Our result also shows that the gate also tunes the contact resistivity which decreases with the increase of the gate voltage. So the whole contact resistance decreases by the increase of current transfer length and the decrease of contact resistivity when the gate voltage increases.

CHAPTER 5: SUMMARY AND PROSPECTIV FUTURE PLAN

5.1 Summary of the Dissertation

In this dissertation, my study on metal contacts on low-dimensional materials has been presented, with a focus on metal contacts on SiNW and MoS₂.

First, the metal contact on SiNW field effect transistors (FETs) was studied with a gate assisted Kelvin structure. SiNW is an example of one-dimensional semiconductor. In this work, I fabricated ambipolar SiNW FETs with Al contacts. The ambipolar behavior of the SiNW FETs and the gate assisted Kelvin structure enabled the measurement of contact properties of electron- and hole-flow at the same contact. We found that the contact performance is significantly affected by the type of carriers that flow in the channel as well as the current direction. Also, an inverter was obtained on a single SiNW.

Then, metal contacts on MoS₂, which is a two-dimensional semiconductor, are studied. In the first part of this work, Ag and Ti contacts on exfoliated MoS₂ flakes are compared. Based on the current-voltage (I-V) measurement, surface morphology and Raman spectroscopy, we found that interface morphology plays an important role on the contact performance in MoS₂ FETs. In the second part of this work, gated assisted contact measurement was carried out on chemical vapor deposited MoS₂. The contact resistance and current crowding were analyzed under different gate bias. All these

findings contribute to understanding the properties and mechanism of metal contact on MoS₂.

5.2 Prospective Future Plan

SiNWs and MoS₂ are good examples of emerging low-dimensional materials. The gate assisted contact measurement can also be applied on other emerging materials to characterize the contacts in electronic devices, to understand the mechanism in such contacts and to reduce contact resistance. As the devices are further scaled down, the issues of metal contacts in the electronic devices are increasingly important. It is important to study the mechanism of the metal contacts on low-dimensional materials.

Furthermore, my work will expand to all aspects of the contacts on the low-dimensional materials. For MoS₂ and other 2D semiconductors (e.g., h-BN and black phosphorus), the details in the contact performance such as the band alignment and the evolution of the band bending under sufficient bias have not been much explored. I will continue the work on the characterization of metal contacts, and try to develop deeper understanding of the modeling of the contacts. I hope my work will lead to understanding the contact mechanism and finding the way to reduce contact resistance or maintain low contact resistance for low-dimensional materials.

Also, I plan to apply the knowledge from my current research to new materials. Black phosphorus, for example, is a good platform to investigate the contacts as well. It attracts quite a lot of attention for the electronic applications for better carrier mobility. I

would like focus on this research and help to enhance the device performance by reducing the contact resistance.

Moreover, because Fermi level pinning not only increases the contact resistance but also decreases the barrier which is needed in photovoltaic and solar cell devices. The Fermi level pinning makes it difficult to form a high barrier between different contacts. In order to improve the efficiency of the photovoltaic devices, it will be equally important to find a way to maintain good energy barriers.

APPENDIX: POLARIZATION OF BI₂TE₃ THIN FILM IN A FLOATING-GATE CAPACITOR STRUCTURE

A.1 Introduction

Topological insulators (TIs) are materials that have an insulator (or semiconductor) bulk and gapless surfaces which are protected by time reversal symmetry.[100] These materials have a Dirac cone at the surface that can be detected by angle resolved photo emission spectroscopy (ARPES).[101, 102] The electrons at the TI surface can be considered as massless Dirac fermions.[103, 104] Therefore, carriers in these surface states have fast response and high mobility.[105] The robustness of the TI surface states is protected by time reversal symmetry and is resistant to external perturbations such as defects and electric field.[106]

Several groups have recently reported the surfaces state analysis and the magneto-electric effects of the TI materials.[107-110] They found that different quantum states can coexist in the surface and can be changed by external magnetic field which breaks the time reversal symmetry. However, these studies were mostly based on theoretical approach, delicate surface characterization method (e.g. ARPES) or scanning tunneling microscopy (STM). There is limited progress in the study of device applications. It would be very important and interesting to study how the TI materials behave in a device structure. We have previously reported a study of high-performance TI nanowire field

effect transistor (FET) in which the TI materials acted as a conducting medium.[111] FETs based on topological crystalline insulator SnTe thin film have also been recently demonstrated.[112] However, the study of floating-gate structure in which TI materials are surrounded by dielectric has not yet been reported. It would be very interesting to see how the TI materials behave with a vertical electric field across them, as well as how they act as an information storage medium.

Information storage is of great interest in microelectronics. It is well recognized that the future information technology relies on novel electrically accessible non-volatile memory (NVM) with high speed and high density.[33] There are several NVM candidates, including ferroelectric NVM, charge-storage memory (e.g., flash memory), molecular memory and resistance random-access memory (RRAM).[113-116] Among them, ferroelectric NVM is very attractive for its low power consumption, fast write / erase and good endurance.¹¹ However, the conventional perovskite ferroelectric materials are disadvantageous for low storage density and high integration cost.[117, 118]

In this work, we fabricated Metal-Oxide-Semiconductor (MOS) capacitors with a Bi_2Te_3 thin film sandwiched by two oxide layers. The Bi_2Te_3 film acts as a “floating gate” similar to the poly-Si floating gate in a FLASH memory. We have studied the polarization of the Bi_2Te_3 thin film for memory application. Such a hybrid MOS structure is very interesting for information storage and can also provide a good platform to study the properties of TI materials.

A.2. Experimental

The schematic of the MOS capacitor structure is shown in Fig. A.1(a). The Bi_2Te_3 film was inserted in between the SiO_2 and Al_2O_3 , forming a metal/ Al_2O_3 / Bi_2Te_3 / SiO_2 / Si (MABOS) capacitor structure. The substrate is low doped (doping concentration about 10^{15} cm^{-3}) n-type Si wafers with 300 nm thermally grown SiO_2 . The fabrication of these MABOS capacitors followed a conventional photolithographic procedure. First, an active area ($100 \mu\text{m} \times 100 \mu\text{m}$, $50 \mu\text{m} \times 50 \mu\text{m}$, $25 \mu\text{m} \times 25 \mu\text{m}$ or $10 \mu\text{m} \times 10 \mu\text{m}$) was defined and etched through a layer of 300 nm SiO_2 thermally grown on n-Si wafers. The wafers were then oxidized at 900°C for 22 minutes to achieve 11 nm dry SiO_2 . The dry oxide is thinned down to 6 nm by 2% HF etch for 60 seconds. Then, atomic layer deposition (ALD) was used to deposit 30 nm Bi_2Te_3 and 30 nm Al_2O_3 on the samples followed by the formation of top Al gate. The extra Bi_2Te_3 , Al_2O_3 , and Al top gate beyond the active region were removed by ion mill before electrical measurement. Finally, the samples were annealed at 300°C in Ar by using rapid thermal annealing (RTA).

The detail ALD conditions for Bi_2Te_3 and Al_2O_3 are as following. The Bi_2Te_3 thin films were synthesized using bismuth trichloride (BiCl_3) and (trimethylsilyl) telluride ($(\text{Me}_3\text{Si})_2\text{Te}$) as chemical ALD precursors. The growth temperature was 170°C . The BiCl_3 precursor was volatilized at a temperature of 140°C and the Te precursor was heated at 45°C . Furthermore 10 sccm of N_2 was used as a carrier gas flow for the precursors. The ALD reaction chamber base pressure was kept at 40 mTorr. The deposition of Al_2O_3 thin film followed a conventional ALD procedure which uses

trimethylaluminum (TMA, $\text{Al}(\text{CH}_3)_3$) and O_2 plasma as precursors. The growth temperature was $300\text{ }^\circ\text{C}$. N_2 was also used as a carrier gas and the ALD reaction chamber base pressure was kept at 20 mTorr.

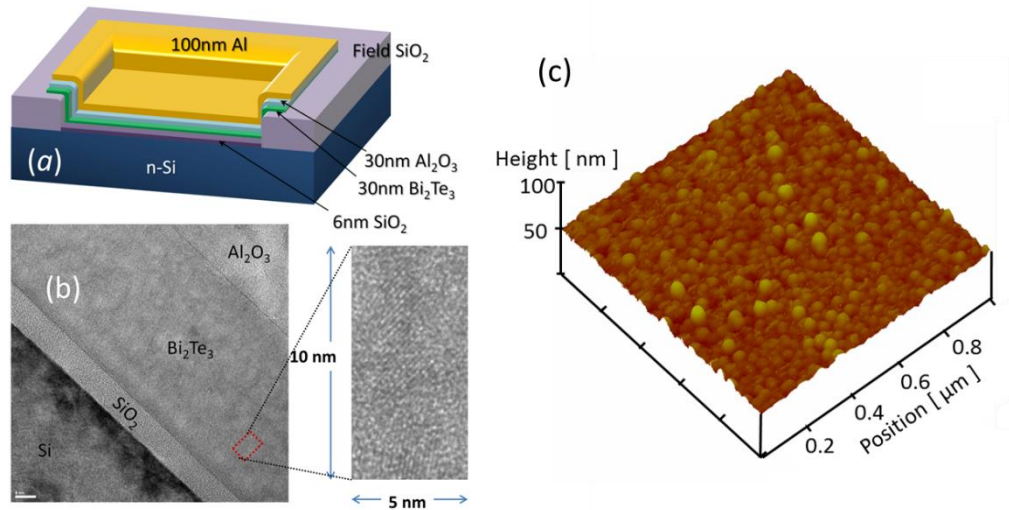


Figure A.1 (a) Schematic of the capacitor with $\text{Al}/\text{Al}_2\text{O}_3/\text{Bi}_2\text{Te}_3/\text{SiO}_2/\text{Si}$ structure. (b) High-resolution transmission electron microscopy (HRTEM) image of the capacitor cross-section. The scale bar is 5 nm in the image. The rectangular HRTEM image ($10\text{ nm} \times 5\text{ nm}$) on the right is an amplification of the Bi_2Te_3 film within the red rectangle on the left image, showing the polycrystalline structure in the film. (c) AFM image of Bi_2Te_3 film grown on SiO_2 with OH-hydroxyl groups by ALD.

The resulting devices were first characterized with the transmission electron microscope (TEM) image of the MOS capacitor cross-section is shown in Fig. A.1(b), indicating that the Bi_2Te_3 is poly-crystalline. Atomic force microscopic (AFM) image of the Bi_2Te_3 film grown by ALD on SiO_2 is shown in Fig. A.1(c). It clear shows that the Bi_2Te_3 is poly-crystalline and the film is uniform with a smooth surface. The whole

process we used is compatible with complementary metal-oxide-semiconductor (CMOS) protocol, which provides a smooth transition to the application in microelectronics.

Capacitance-voltage (C-V) characterization was carried out by using an impedance analyzer and a vacuum probe station. During the measurement, the samples were kept in 4×10^{-7} Torr vacuum.

A.3 Results and discussion

Fig. A. 2 shows the C-V characteristics of MABOS capacitors with an area of $100 \mu\text{m} \times 100 \mu\text{m}$. The C-V measurement was carried out at 1 MHz. These capacitors exhibit a hysteresis in C-V characteristics at room temperature. The hysteresis has a same direction of ferroelectric base capacitors.[119, 120] As shown in Fig. A.2(a), the flat-band voltage (V_{FB}) of the C-V curve shifted to positive as the gate voltage was scanned from negative to positive. The hysteresis is larger when a larger range of gate voltage was scanned. But the hysteresis did not disappear even during a low voltage scan. The same hysteresis also shows in the MABOS capacitors with smaller area.

The hysteresis of MABOS capacitors is different from the hysteresis of a floating-gate memory cell. First, this hysteresis shift is opposite to that of a floating-gate memory device based on charge-trapping mechanism.[121, 122] As shown in inset of Fig. A.2(a), in a floating-gate memory cell, positive charges (holes) will tunnel from Si into the floating gate after gate voltage sweeps from negative to positive, resulting in V_{FB} shift to negative. Second, the hysteresis of MABOS capacitors exists in all sweep ranges, even in a small voltage sweep range from -3V to 3V. This is different from the charge-trapping

devices of which the hysteresis is present only when gate voltage exceeds tunneling threshold voltage.[121, 123]

In these MABOS capacitor devices, 6nm SiO₂ is thick enough to prevent the electron/hole tunneling between the Bi₂Te₃ and Si at such a low electric field. Even in the worst case that a small amount of charges tunnel through the 6nm SiO₂, the hysteresis shift should be in the opposite direction as mentioned above. Also, the Al₂O₃ layer is about 30nm, thick enough to block the charge transfer between Bi₂Te₃ and the gate metal. Therefore, the hysteresis shift must be resulted by the polarization of Bi₂Te₃ film. In detail, the polarization is a result of charge accumulation on the two surfaces of Bi₂Te₃: the electrons and holes within the Bi₂Te₃ film are separated and driven by the electric field; and then, they are accumulated on either surfaces of the Bi₂Te₃ film, building an internal electrical field in the opposite direction to the external electrical field. This is quite similar to the polarization of metals and semiconductors in an electrical field.

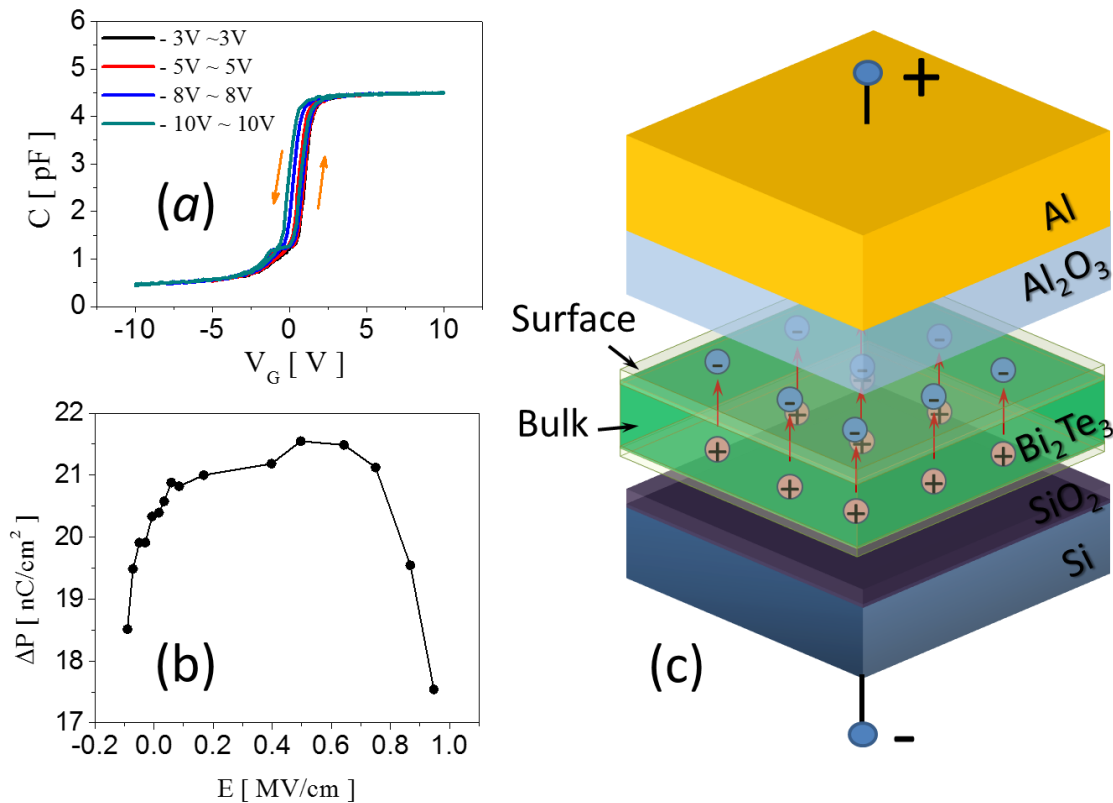


Figure A.2 (a) Capacitance-Voltage (C-V) characteristics of the Bi₂Te₃ capacitor structure at 1 MHz with different voltage sweep ranges. The area of the capacitor is 100 $\mu\text{m} \times 100 \mu\text{m}$. (b) The polarization difference changes versus the applied voltage. (c) Illustration of the charge separation and polarization of Bi₂Te₃ when an external field is applied.

The movement of carriers is much faster than the displacement of atoms/ions in the ferroelectric materials. The polarization shown in the C-V hysteresis is a result of accumulation of charge carriers on the surfaces. Unlike ferroelectrics where the polarization is due to the displacement of ions in the crystal, the polarization of Bi₂Te₃ film is induced by the accumulation of carriers (electrons and holes). Therefore, the polarization of the Bi₂Te₃ film in the MABOS structure should be much faster than that of normal ferroelectric films. Also, compared to the ion displacement in conventional

ferroelectric materials, the electron movement should have less damage on the materials, leading to better device endurance.

To extract the polarization of Bi_2Te_3 , we estimated the capacitance of dielectric layers based on the conventional model of MOS capacitor at high frequency. We can consider the polarized Bi_2Te_3 as a parallel-plate capacitor with opposite polarized carriers (electrons or holes) on each surface. So, the capacitance of insulating layers can be obtained from the capacitance in accumulation region ($100 \mu\text{m} \times 100 \mu\text{m}$ capacitors), that is:

$$C_{\text{INS}} = 4.6 \text{ pF} \quad (\text{A.1})$$

Because the capacitance was measured with a small signal method, the transient polarized charges do not contribute to the total capacitance. However, this charge separation (or polarization) shift V_{FB} of the MABOS capacitor to negative or positive directions so that the hysteresis in the C-V measurement appears. The value of the applied gate voltages at the same capacitance in forward and reverse sweep directions can be obtained. As discussed above, the difference between these two gate voltage values (ΔV_G) is due to the difference in polarization (ΔP) of Bi_2Te_3 between the two sweep directions. Their relationship can be expressed as:

$$\Delta V_G = \frac{\Delta Q_P}{C_{\text{Bi}_2\text{Te}_3}} = \frac{\Delta P \cdot A}{C_{\text{Bi}_2\text{Te}_3}}, \quad (\text{A.2})$$

Here, ΔQ_P stands for the polarized charge difference, A for area of the capacitor, and the capacitance of Bi_2Te_3 ($C_{\text{Bi}_2\text{Te}_3} = 6.07 \text{ pF}$) is calculated from the total insulator

capacitance which is assumed to be the total capacitance of SiO₂, Bi₂Te₃ and Al₂O₃ in serial.

Fig. A.2(b) shows the ΔP at different electric field. To calculate the electric field, a standard MOS capacitor with the same insulating layer capacitance (the capacitances of Al₂O₃, Bi₂Te₃ and SiO₂ in series, ≈ 4.6 pF) and doping concentration (1×10^{15} cm⁻³) as the measured capacitors was designed for simulation. The applied voltage of the standard MOS capacitor is recorded at the same value of capacitance measured in the experiment. This recorded voltage is over flat band voltage, i.e. gate voltage (V_G) - flat band voltage (V_{FB}). The net voltage drop across Bi₂Te₃, V_{BT} , which is partial of ($V_G - V_{FB}$), can be extracted from the serial capacitor model. The electric field is V_{BT} divided by the thickness of Bi₂Te₃. We extract the ΔP in depletion-accumulation transition region when the capacitance changes dramatic with applied voltage. In the depletion or accumulation region the capacitance changes little with the applied voltage, the extraction of the ΔP would be inaccurate. The result indicates that the ΔP is largest around the flat-band voltage when the when the voltage drop across Bi₂Te₃ is small..

The memory window ΔV_{FB} is the ΔV_G when the capacitance is equal to the flat band capacitance (C_{FB}). C_{FB} can be expressed as:[124]

$$C_{FB} = \frac{C_{SFB} \cdot C_{INS}}{C_{SFB} + C_{INS}} = 2.92 \text{ pF} \quad (\text{A.3a})$$

$$C_{SFB} = \frac{\epsilon_S \epsilon_0 A}{\lambda_n} = A \sqrt{\frac{q^2 N_D \epsilon_S \epsilon_0}{kT}} = 8 \times 10^{-12} \text{ F} \quad (\text{A.3b})$$

where the flat-band condition capacitance of Si (C_{SFB}) is the capacitance of Si (C_s) at flat-band condition, λ_n is the depletion width in Si at flat-band condition, A is the area of the capacitor, N_D is the doping concentration (10^{15} cm^{-3} in our Si wafer), ϵ_s and ϵ_0 are Si relative permittivity and vacuum permittivity, respectively.

We have also performed temperature-dependent C-V characterization to study the polarization formation. The sample was measured at temperatures from 80K to 290K. As shown in Fig. A.3, the hysteresis decreases as the temperature decreases. Below 250K, the hysteresis is very small, almost negligible (Fig. A.3(d)). At each temperature, the C-V curves measured at different frequencies are approximately the same. Also, the hysteresis of the C-V curves at different frequencies is the same. This indicates that there is negligible frequency-dependence in the C-V measurement when frequency ≤ 1 MHz. In addition, the devices have been repeatedly tested for many times over a long period of duration (> 6 months). The measured results are very reproducible in all these tests. The devices exhibit better programming/erasing characteristics than conventional poly-Si Flash memory (1×10^6 cycles). This is because the polarization of surface state in Bi_2Te_3 causes much less damage than hot-electron injection in conventional Flash memory cells.

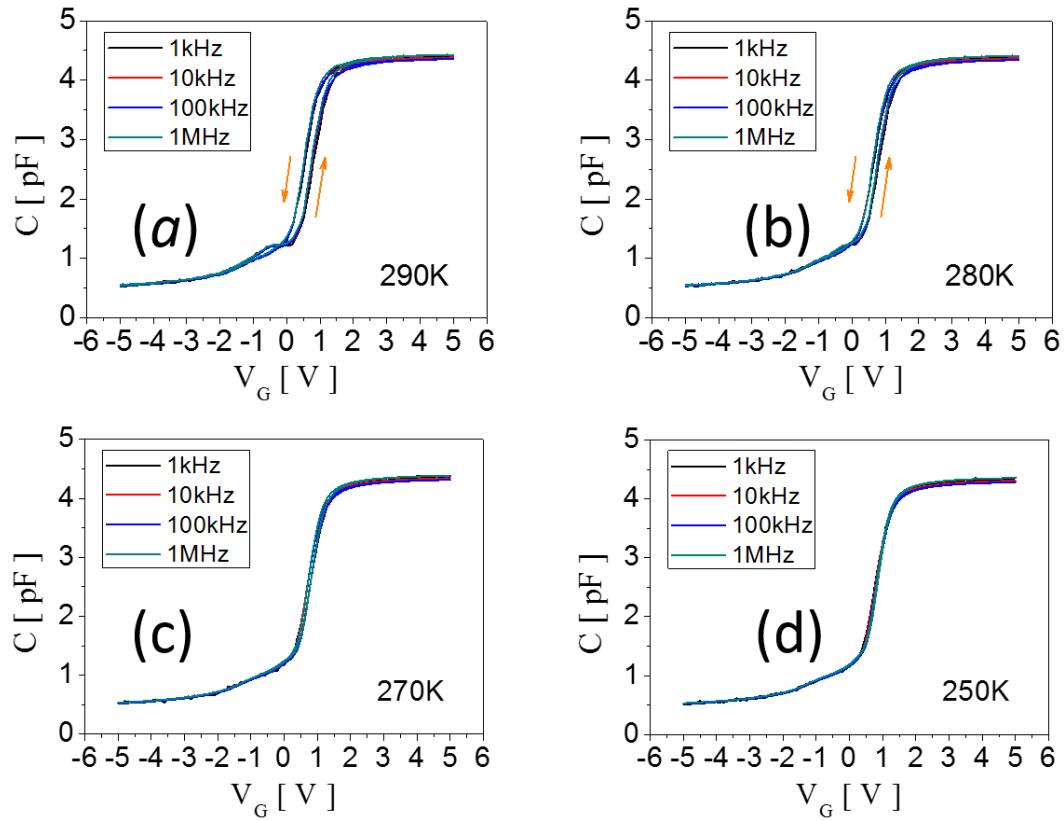


Figure A.3 C-V characteristics the Bi_2Te_3 capacitor structure at different frequencies (1 kHz to 1 MHz) at different temperatures: (a) 290K, (b) 280K, (c) 270K and (d) 250K. The hysteresis shift decreases as the temperature decreases.

Fig. A.4(a) showed that ΔP changes with electric field at different temperatures. The ΔP is eliminated when the temperature decreases. But the largest value of ΔP always shows around flat-band voltage. Fig A.4(b) shows the memory window (ΔV_{FB}) changes versus the temperature.

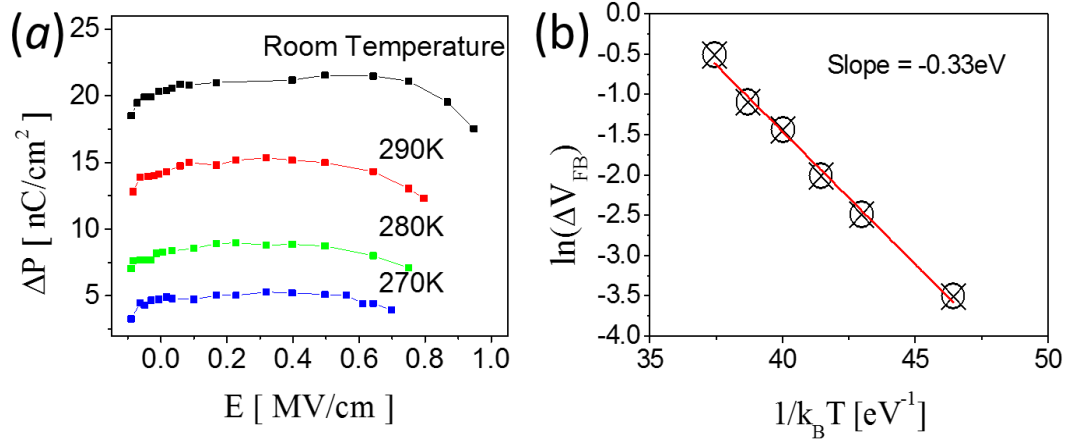


Figure A.4 (a) Polarization difference at vs. applied voltage different temperatures. (b) Memory window vs. temperature. The memory window is shrunk as the temperature decreases, indicating that the remnant polarization becomes smaller at lower temperature. The memory window is fitted as an exponential function of $1/k_B T$ ($k_B T$ is the thermal activation energy), agreeing well with both the linear- and log-scale experimental data. The activation energy is 0.33eV according to the fitting.

The quantitative analysis of polarization of Bi_2Te_3 indicates thermal activation of the surface carriers is the origin of polarization. In this case, ΔV_{FB} can be written as:

$$\Delta V_{FB} = \frac{A\Delta P}{C_{\text{Bi}_2\text{Te}_3}} = \frac{A}{C_{\text{Bi}_2\text{Te}_3}} \Delta P_0 e^{\frac{q\phi_B}{kT}}, \quad (\text{A.4a})$$

$$\ln \Delta V_{FB} = C_0 + \frac{q\phi_B}{k_B T}, \quad (\text{A.4b})$$

where ΔP_0 is a fitting parameter, and $q\phi_B$ is the activation energy. Fig. A.4(b) clearly shows the ΔV_{FB} is exponential to $1/k_B T$. We can get $q\phi_B$ equals to 0.33eV from linear fitting of $\ln(\Delta V_{FB})$ versus $1/k_B T$. This relationship between ΔV_{FB} and temperature indicates the carriers were thermal activated from surface state to bulk, and then moved and accumulated on the other surface when an external electric field was applied.

In addition, we have also fabricated and measured MOS capacitors with different thickness of Bi_2Te_3 . We found that MOS capacitors with Bi_2Te_3 thinner than 15nm did not exhibit significant hysteresis. It seems that the thin Bi_2Te_3 in the capacitor behaves as a conductor. On the other hand, thick Bi_2Te_3 will significantly decrease the electric field across it, resulting in small polarization and memory window.

A.4 Conclusion

We have fabricated and characterized floating-gate-like MOS capacitors with topological insulator (Bi_2Te_3) thin film sandwiched between insulating dielectric layers. The capacitors exhibited ferroelectric-like hysteresis. We have fully characterized and analyzed the hysteresis, and confirmed that it was a result of the polarization of Bi_2Te_3 under vertical electric field. Also, the polarization was identified as a result of carrier separation under vertical electric field, which is different with ferroelectrics. The thermal activation energy for the carriers (electron and hole) to separate and accumulate at the top and bottom surface of Bi_2Te_3 was extracted to be 0.33eV. Due to the fast polarization speed and excellent endurance insured by the protected surface states, as well as the CMOS compatibility, the Bi_2Te_3 embedded MOS structures are very interesting for memory application. Besides, this work demonstrated that the floating-gate capacitor structure is an effective platform to study the properties of topological insulator thin films.

REFERENCES

- [1] H. J. Fan, P. Werner, and M. Zacharias, "Semiconductor nanowires: From self-organization to patterned growth," *Small*, vol. 2, pp. 700-717, Jun 2006.
- [2] Y. Cui and C. M. Lieber, "Functional nanoscale electronic devices assembled using silicon nanowire building blocks," *Science*, vol. 291, pp. 851-853, Feb 2 2001.
- [3] Y. Cui, Z. Zhong, D. Wang, W. U. Wang, and C. M. Lieber, "High Performance Silicon Nanowire Field Effect Transistors," *Nano Lett.*, vol. 3, pp. 149-152, 2003/02/01 2003.
- [4] M. P. Anantram and F. Léonard, "Physics of carbon nanotube electronic devices," *Reports on Progress in Physics*, vol. 69, p. 507, 2006.
- [5] S. J. Tans, A. R. M. Verschueren, and C. Dekker, "Room-temperature transistor based on a single carbon nanotube," *Nature*, vol. 393, pp. 49-52, 05/07/print 1998.
- [6] K. S. Novoselov, V. I. Falko, L. Colombo, P. R. Gellert, M. G. Schwab, and K. Kim, "A roadmap for graphene," *Nature*, vol. 490, pp. 192-200, 10/11/print 2012.
- [7] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov, "Electric Field Effect in Atomically Thin Carbon Films," *Science*, vol. 306, pp. 666-669, October 22, 2004 2004.
- [8] L. Liao, Y.-C. Lin, M. Bao, R. Cheng, J. Bai, Y. Liu, Y. Qu, K. L. Wang, Y. Huang, and X. Duan, "High-speed graphene transistors with a self-aligned nanowire gate," *Nature*, vol. 467, pp. 305-308, 09/16/2010 2010.
- [9] B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, and A. Kis, "Single-layer MoS₂ transistors," *Nat. Nanotechnol.*, vol. 6, pp. 147-150, Mar 2011.
- [10] S. Z. Butler, S. M. Hollen, L. Cao, Y. Cui, J. A. Gupta, H. R. Gutiérrez, T. F. Heinz, S. S. Hong, J. Huang, A. F. Ismach, E. Johnston-Halperin, M. Kuno, V. V. Plashnitsa, R. D. Robinson, R. S. Ruoff, S. Salahuddin, J. Shan, L. Shi, M. G. Spencer, M. Terrones, W. Windl, and J. E. Goldberger, "Progress, Challenges, and Opportunities in Two-Dimensional Materials Beyond Graphene," *ACS Nano*, vol. 7, pp. 2898-2926, 2013/04/23 2013.

- [11] D. Jariwala, V. K. Sangwan, L. J. Lauhon, T. J. Marks, and M. C. Hersam, "Emerging Device Applications for Semiconducting Two-Dimensional Transition Metal Dichalcogenides," *ACS Nano*, vol. 8, pp. 1102-1120, 2014/02/25 2014.
- [12] D. Hisamoto, W.-C. Lee, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo, E. Anderson, T.-J. King, J. Bokor, and C. Hu, "FinFET-a self-aligned double-gate MOSFET scalable to 20 nm," *IEEE Trans. Electron Devices*, vol. 47, pp. 2320-2325, 2000.
- [13] T. Böker, R. Severin, A. Müller, C. Janowitz, R. Manzke, D. Voß, P. Krüger, A. Mazur, and J. Pollmann, "Band structure of MoS₂, MoSe₂, and α -MoTe₂: Angle-resolved photoelectron spectroscopy and ab initio calculations," *Phys Rev B*, vol. 64, p. 235305, 2001.
- [14] A. Kuc, N. Zibouche, and T. Heine, "Influence of quantum confinement on the electronic structure of the transition metal sulfide TS₂," *Phys Rev B*, vol. 83, p. 245213, 06/30/ 2011.
- [15] S. Lebegue and O. Eriksson, "Electronic structure of two-dimensional crystals from ab initio theory," *Phys Rev B*, vol. 79, p. 115409, 03/11/ 2009.
- [16] H. Liu, A. T. Neal, Z. Zhu, Z. Luo, X. Xu, D. Tománek, and P. D. Ye, "Phosphorene: An Unexplored 2D Semiconductor with a High Hole Mobility," *ACS Nano*, vol. 8, pp. 4033-4041, 2014/04/22 2014.
- [17] Y. Du, C. Ouyang, S. Shi, and M. Lei, "Ab initio studies on atomic and electronic structures of black phosphorus," *J. Appl. Phys.*, vol. 107, pp. -, 2010.
- [18] V. Tran, R. Soklaski, Y. Liang, and L. Yang, "Layer-controlled band gap and anisotropic excitons in few-layer black phosphorus," *Phys Rev B*, vol. 89, p. 235319, 06/26/ 2014.
- [19] H.-Y. Chang, S. Yang, J. Lee, L. Tao, W.-S. Hwang, D. Jena, N. Lu, and D. Akinwande, "High-Performance, Highly Bendable MoS₂ Transistors with High-K Dielectrics for Flexible Low-Power Systems," *ACS Nano*, vol. 7, pp. 5446-5452, 2013/06/25 2013.
- [20] G.-H. Lee, Y.-J. Yu, X. Cui, N. Petrone, C.-H. Lee, M. S. Choi, D.-Y. Lee, C. Lee, W. J. Yoo, K. Watanabe, T. Taniguchi, C. Nuckolls, P. Kim, and J. Hone, "Flexible and Transparent MoS₂ Field-Effect Transistors on Hexagonal Boron Nitride-Graphene Heterostructures," *ACS Nano*, vol. 7, pp. 7931-7936, 2013/09/24 2013.
- [21] C. Kocabas, S. Dunham, Q. Cao, K. Cimino, X. N. Ho, H. S. Kim, D. Dawson, J. Payne, M. Stuenkel, H. Zhang, T. Banks, M. Feng, S. V. Rotkin, and J. A. Rogers, "High-Frequency Performance of Submicrometer Transistors That Use Aligned Arrays of Single-Walled Carbon Nanotubes," *Nano Lett.*, vol. 9, pp. 1937-1943, May 2009.

- [22] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, M. I. Katsnelson, I. V. Grigorieva, S. V. Dubonos, and A. A. Firsov, "Two-dimensional gas of massless Dirac fermions in graphene," *Nature*, vol. 438, pp. 197-200, Nov 2005.
- [23] Y. Q. Wu, K. A. Jenkins, A. Valdes-Garcia, D. B. Farmer, Y. Zhu, A. A. Bol, C. Dimitrakopoulos, W. J. Zhu, F. N. Xia, P. Avouris, and Y. M. Lin, "State-of-the-Art Graphene High-Frequency Electronics," *Nano Lett.*, vol. 12, pp. 3062-3067, Jun 2012.
- [24] E. W. Hill, A. K. Geim, K. Novoselov, F. Schedin, and P. Blake, "Graphene spin valve devices," *IEEE Trans. Magn.*, vol. 42, pp. 2694-2696, Oct 2006.
- [25] N. Tombros, C. Jozsa, M. Popinciuc, H. T. Jonkman, and B. J. van Wees, "Electronic spin transport and spin precession in single graphene layers at room temperature," *Nature*, vol. 448, pp. 571-U4, Aug 2007.
- [26] G. Balasubramanian, P. Neumann, D. Twitchen, M. Markham, R. Kolesov, N. Mizuochi, J. Isoya, J. Achard, J. Beck, J. Tissler, V. Jacques, P. R. Hemmer, F. Jelezko, and J. Wrachtrup, "Ultralong spin coherence time in isotopically engineered diamond," *Nat. Mater.*, vol. 8, pp. 383-387, May 2009.
- [27] A. Splendiani, L. Sun, Y. Zhang, T. Li, J. Kim, C.-Y. Chim, G. Galli, and F. Wang, "Emerging Photoluminescence in Monolayer MoS₂," *Nano Lett.*, vol. 10, pp. 1271-1275, 2010/04/14 2010.
- [28] Y. Ding, Y. Wang, J. Ni, L. Shi, S. Shi, and W. Tang, "First principles study of structural, vibrational and electronic properties of graphene-like MX₂ (M=Mo, Nb, W, Ta; X=S, Se, Te) monolayers," *Physica B: Condensed Matter*, vol. 406, pp. 2254-2260, 5/15/ 2011.
- [29] A. Rycerz, J. Tworzydło, and C. W. J. Beenakker, "Valley filter and valley valve in graphene," *Nature Phys.*, vol. 3, pp. 172-175, Mar 2007.
- [30] J. L. Garcia-Pomar, A. Cortijo, and M. Nieto-Vesperinas, "Fully valley-polarized electron beams in graphene," *Phys. Rev. Lett.*, vol. 100, p. 4, Jun 2008.
- [31] H. L. Zeng, J. F. Dai, W. Yao, D. Xiao, and X. D. Cui, "Valley polarization in MoS₂ monolayers by optical pumping," *Nat. Nanotechnol.*, vol. 7, pp. 490-493, Aug 2012.
- [32] T. Cao, G. Wang, W. P. Han, H. Q. Ye, C. R. Zhu, J. R. Shi, Q. Niu, P. H. Tan, E. Wang, B. L. Liu, and J. Feng, "Valley-selective circular dichroism of monolayer molybdenum disulphide," *Nat. Commun.*, vol. 3, p. 5, Jun 2012.
- [33] "ITRS 2013," ITRS 2013.

- [34] F. J. Himpsel, G. Hollinger, and R. A. Pollak, "DETERMINATION OF THE FERMI-LEVEL PINNING POSITION AT SI(111) SURFACES," Phys Rev B, vol. 28, pp. 7014-7018, 1983.
- [35] F. Leonard and A. A. Talin, "Electrical contacts to one- and two-dimensional nanomaterials," Nat Nano, vol. 6, pp. 773-783, 12//print 2011.
- [36] F. Leonard and J. Tersoff, "Role of Fermi-level pinning in nanotube Schottky diodes," Phys. Rev. Lett., vol. 84, pp. 4693-4696, May 2000.
- [37] S. Das, H.-Y. Chen, A. V. Penumatcha, and J. Appenzeller, "High Performance Multilayer MoS₂ Transistors with Scandium Contacts," Nano Lett., vol. 13, pp. 100-105, 2013/01/09 2012.
- [38] C. Gong, L. Colombo, R. M. Wallace, and K. Cho, "The Unusual Mechanism of Partial Fermi Level Pinning at Metal–MoS₂ Interfaces," Nano Lett., vol. 14, pp. 1714-1720, 2014/04/09 2014.
- [39] ITRS 2011, Emerging Research Devices.
- [40] A. D. Franklin and Z. Chen, "Length scaling of carbon nanotube transistors," Nat. Nanotechnol., vol. 5, pp. 858-862, 12//print 2010.
- [41] J. Appenzeller, J. Knoch, M. T. Bjork, H. Riel, H. Schmid, and W. Riess, "Toward Nanowire Electronics," Electron Devices, IEEE Transactions on, vol. 55, pp. 2827-2845, 2008.
- [42] J.-P. Colinge, C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, P. Razavi, B. O'Neill, A. Blake, M. White, A.-M. Kelleher, B. McCarthy, and R. Murphy, "Nanowire transistors without junctions," Nat. Nanotechnol., vol. 5, pp. 225-229, 2010.
- [43] S.-M. Koo, M. D. Edelstein, Q. Li, C. A. Richter, and E. M. Vogel, "Silicon nanowires as enhancement-mode Schottky barrier field-effect transistors," Nanotechnology, vol. 16, p. 1482, 2005.
- [44] J. J. Ke, K. T. Tsai, Y. A. Dai, and J. H. He, "Contact transport of focused ion beam-deposited Pt to Si nanowires: From measurement to understanding," Appl. Phys. Lett., vol. 100, pp. -, 2012.
- [45] A. Chaudhry, V. Ramamurthi, E. Fong, and M. S. Islam, "Ultra-low contact resistance of epitaxially interfaced bridged silicon nanowires," Nano Lett., vol. 7, pp. 1536-1541, Jun 2007.

- [46] S. E. Mohny, Y. Wang, M. A. Cabassi, K. K. Lew, S. Dey, J. M. Redwing, and T. S. Mayer, "Measuring the specific contact resistance of contacts to semiconductor nanowires," *Solid-State Electron.*, vol. 49, pp. 227-232, Feb 2005.
- [47] C. A. Richter, H. D. Xiong, Z. Xiaoxiao, W. Wang, V. M. Stanford, W.-K. Hong, L. Takhee, D. E. Ioannou, and L. Qiliang, "Metrology for the Electrical Characterization of Semiconductor Nanowires," *Electron Devices, IEEE Transactions on*, vol. 55, pp. 3086-3095, 2008.
- [48] L. Choi, B. H. Hong, Y. C. Jung, K. H. Cho, K. H. Yeo, D.-W. Kim, G. Y. Jin, K. S. Oh, W.-S. Lee, S.-H. Song, J.-S. Rieh, D. M. Whang, and S. W. Hwang, "Extracting Mobility Degradation and Total Series Resistance of Cylindrical Gate-All-Around Silicon Nanowire Field-Effect Transistors," *Electron Device Letters, IEEE*, vol. 30, pp. 665-667, 2009.
- [49] L. K. Mak, C. M. Rogers, and D. C. Northrop, "Specific contact resistance measurements on semiconductors," *Journal of Physics E: Scientific Instruments*, vol. 22, p. 317, 1989.
- [50] T. Roy, M. Tosun, J. S. Kang, A. B. Sachid, S. B. Desai, M. Hettick, C. C. Hu, and A. Javey, "Field-Effect Transistors Built from All Two-Dimensional Material Components," *ACS Nano*, vol. 8, pp. 6259-6264, 2014/06/24 2014.
- [51] H. Li, Z. Yin, Q. He, H. Li, X. Huang, G. Lu, D. W. H. Fam, A. I. Y. Tok, Q. Zhang, and H. Zhang, "Fabrication of Single- and Multilayer MoS₂ Film-Based Field-Effect Transistors for Sensing NO at Room Temperature," *Small*, vol. 8, pp. 63-67, 2012.
- [52] L. Wang, Y. Wang, J. I. Wong, T. Palacios, J. Kong, and H. Y. Yang, "Functionalized MoS₂ Nanosheet-Based Field-Effect Biosensor for Label-Free Sensitive Detection of Cancer Marker Proteins in Solution," *Small*, vol. 10, pp. 1101-1105, 2014.
- [53] R. S. Sundaram, M. Engel, A. Lombardo, R. Krupke, A. C. Ferrari, P. Avouris, and M. Steiner, "Electroluminescence in Single Layer MoS₂," *Nano Lett.*, 2013.
- [54] Z. Y. Yin, H. Li, L. Jiang, Y. M. Shi, Y. H. Sun, G. Lu, Q. Zhang, X. D. Chen, and H. Zhang, "Single-Layer MoS₂ Phototransistors," *ACS Nano*, vol. 6, pp. 74-80, Jan 2012.
- [55] J. Yoon, W. Park, G.-Y. Bae, Y. Kim, H. S. Jang, Y. Hyun, S. K. Lim, Y. H. Kahng, W.-K. Hong, B. H. Lee, and H. C. Ko, "Highly Flexible and Transparent Multilayer MoS₂ Transistors with Graphene Electrodes," *Small*, vol. 9, pp. 3295-3300, 2013.
- [56] W.-Y. Lu and Y. Taur, "On the scaling limit of ultrathin SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 53, pp. 1137-1141, 2006.

- [57] S. Das and J. Appenzeller, "Where Does the Current Flow in Two-Dimensional Layered Systems?," *Nano Lett.*, vol. 13, pp. 3396-3402, 2013/07/10 2013.
- [58] W. Zhu, T. Low, Y.-H. Lee, H. Wang, D. B. Farmer, J. Kong, F. Xia, and P. Avouris, "Electronic transport and device prospects of monolayer molybdenum disulphide grown by chemical vapour deposition," *Nat Commun*, vol. 5, p. 3087, 01/17/online 2014.
- [59] M. Y. Chan, K. Komatsu, S.-L. Li, Y. Xu, P. Darmawan, H. Kuramochi, S. Nakaharai, A. Aparecido-Ferreira, K. Watanabe, T. Taniguchi, and K. Tsukagoshi, "Suppression of thermally activated carrier transport in atomically thin MoS₂ on crystalline hexagonal boron nitride substrates," *Nanoscale*, vol. 5, pp. 9572-9576, 2013.
- [60] S.-W. Min, H. S. Lee, H. J. Choi, M. K. Park, T. Nam, H. Kim, S. Ryu, and S. Im, "Nanosheet thickness-modulated MoS₂ dielectric property evidenced by field-effect transistor performance," *Nanoscale*, vol. 5, pp. 548-551, 2013.
- [61] S. Das, A. Prakash, R. Salazar, and J. Appenzeller, "Toward Low-Power Electronics: Tunneling Phenomena in Transition Metal Dichalcogenides," *ACS Nano*, vol. 8, pp. 1681-1689, 2014/02/25 2014.
- [62] S. McDonnell, R. Addou, C. Buie, R. M. Wallace, and C. L. Hinkle, "Defect-Dominated Doping and Contact Resistance in MoS₂," *ACS Nano*, vol. 8, pp. 2880-2888, 2014/03/25 2014.
- [63] S. Chuang, C. Battaglia, A. Azcatl, S. McDonnell, J. S. Kang, X. Yin, M. Tosun, R. Kapadia, H. Fang, R. M. Wallace, and A. Javey, "MoS₂ P-type Transistors and Diodes Enabled by High Work Function MoO_x Contacts," *Nano Lett.*, vol. 14, pp. 1337-1342, 2014/03/12 2014.
- [64] Y. Du, L. Yang, J. Zhang, H. Liu, K. Majumdar, P. D. Kirsch, and P. D. Ye, "MoS₂ Field-Effect Transistors With Graphene/Metal Heterocontacts," *IEEE Electron Device Lett.*, vol. 35, pp. 599-601, 2014.
- [65] S. C. Lim, J. H. Jang, D. J. Bae, G. H. Han, S. Lee, I.-S. Yeo, and Y. H. Lee, "Contact resistance between metal and carbon nanotube interconnects: Effect of work function and wettability," *Appl. Phys. Lett.*, vol. 95, pp. -, 2009.
- [66] W. Liu, J. Kang, D. Sarkar, Y. Khatami, D. Jena, and K. Banerjee, "Role of Metal Contacts in Designing High-Performance Monolayer n-Type WSe₂ Field Effect Transistors," *Nano Lett.*, vol. 13, pp. 1983-1990, 2013/05/08 2013.
- [67] U. Becker, K. M. Rosso, R. Weaver, M. Warren, and M. F. Hochella, "Metal island growth and dynamics on molybdenite surfaces," *Geochim. Cosmochim. Acta*, vol. 67, pp. 923-934, Mar 2003.

- [68] L. Wei, K. Jiahao, C. Wei, D. Sarkar, Y. Khatami, D. Jena, and K. Banerjee, "High-performance few-layer-MoS₂ field-effect-transistor with record low contact-resistance," in Electron Devices Meeting (IEDM), 2013 IEEE International, 2013, pp. 19.4.1-19.4.4.
- [69] B. W. H. Baugher, H. O. H. Churchill, Y. Yang, and P. Jarillo-Herrero, "Intrinsic Electronic Transport Properties of High-Quality Monolayer and Bilayer MoS₂," *Nano Lett.*, vol. 13, pp. 4212-4216, 2013/09/11 2013.
- [70] H. Liu, M. Si, Y. Deng, A. T. Neal, Y. Du, S. Najmaei, P. M. Ajayan, J. Lou, and P. D. Ye, "Switching Mechanism in Single-Layer Molybdenum Disulfide Transistors: An Insight into Current Flow across Schottky Barriers," *ACS Nano*, vol. 8, pp. 1031-1038, 2014/01/28 2013.
- [71] J. Kang, W. Liu, D. Sarkar, D. Jena, and K. Banerjee, "Computational Study of Metal Contacts to Monolayer Transition-Metal Dichalcogenide Semiconductors," *Phys. Rev. X*, vol. 4, p. 031005, 07/14/ 2014.
- [72] H. B. Michaelson, "The work function of the elements and its periodicity," *J. Appl. Phys.*, vol. 48, pp. 4729-4733, 1977.
- [73] Y. Guo, Y. Han, J. Li, A. Xiang, X. Wei, S. Gao, and Q. Chen, "Study on the Resistance Distribution at the Contact between Molybdenum Disulfide and Metals," *ACS Nano*, vol. 8, pp. 7771-7779, 2014/08/26 2014.
- [74] H. Yuan, A. Badwan, C. A. Richter, H. Zhu, O. Kirillov, D. E. Ioannou, and Q. Li, "Gate assisted Kelvin test structure to measure the electron and hole flows at the same nanowire contacts," *Appl. Phys. Lett.*, vol. 105, p. 133513, 2014.
- [75] W. T. Lynch and N. K. K., "A Tester For The Contact Resistivity Of Self-Aligned Silicides," *IEEE International Electron Device Meeting Digest*, pp. 352-355, 1988.
- [76] X. Zhu, Q. Li, D. E. Ioannou, D. Gu, J. Bonevich, E., H. Baumgart, J. Suehle, S., and C. A. Richter, "Fabrication, characterization and simulation of high performance Si nanowire-based non-volatile memory cells," *Nanotechnology*, vol. 22, p. 254020, 2011.
- [77] J. R. Heath and M. A. Ratner, "Molecular Electronics," *Physics Today*, vol. 56, p. 43, 2003.
- [78] Q. Li, S.-M. Koo, C. A. Richter, M. D. Edelstein, J. E. Bonevich, J. J. Kopanski, J. S. Suehle, and E. M. Vogel, "Precise Alignment of Single Nanowires and Fabrication of Nanoelectromechanical Switch and Other Test Structures," *Nanotechnology, IEEE Transactions on*, vol. 6, pp. 256-262, 2007.

- [79] H. H. Berger, "Models for contacts to planar devices," *Solid-State Electron.*, vol. 15, pp. 145-158, 2// 1972.
- [80] C. Ortiz, D. Mathiot, C. Dubois, and R. Jerisian, "Diffusion of low-dose implanted aluminum in silicon in inert and dry O₂ ambient," *J. Appl. Phys.*, vol. 87, pp. 2661-2663, 2000.
- [81] D. A. Antoniadis and I. Moskowitz, "Diffusion of substitutional impurities in silicon at short oxidation times: An insight into point defect kinetics," *J. Appl. Phys.*, vol. 53, pp. 6788-6796, 1982.
- [82] J.-P. Colinge, "Multiple-gate SOI MOSFETs," *Solid-State Electron.*, vol. 48, pp. 897-905, 2004.
- [83] Q. Li, X. Zhu, Y. Yang, D. E. Ioannou, H. D. Xiong, D.-W. Kwon, J. S. Suehle, and C. A. Richter, "The large-scale integration of high-performance silicon nanowire field effect transistors," *Nanotechnology*, vol. 20, p. 415202, 2009.
- [84] H. Li, Q. Zhang, C. C. R. Yap, B. K. Tay, T. H. T. Edwin, A. Olivier, and D. Baillargeat, "From Bulk to Monolayer MoS₂: Evolution of Raman Scattering," *Adv. Funct. Mater.*, vol. 22, pp. 1385-1390, 2012.
- [85] I. Horcas, R. Fernández, J. M. Gómez-Rodríguez, J. Colchero, J. Gómez-Herrero, and A. M. Baro, "WSXM: A software for scanning probe microscopy and a tool for nanotechnology," *Rev Sci Instrum*, vol. 78, p. 013705, 2007.
- [86] C. Gong, C. Huang, J. Miller, L. Cheng, Y. Hao, D. Cobden, J. Kim, R. S. Ruoff, R. M. Wallace, K. Cho, X. Xu, and Y. J. Chabal, "Metal Contacts on Physical Vapor Deposited Monolayer MoS₂," *ACS Nano*, vol. 7, pp. 11350-11357, 2013/12/23 2013.
- [87] S. Y. Li, J. A. Rodriguez, J. Hrbek, H. H. Huang, and G. Q. Xu, "Chemical and electronic properties of silver atoms supported on sulfur and molybdenum sulfide surfaces," *Surf. Sci.*, vol. 395, pp. 216-228, Jan 1998.
- [88] H. J. Conley, B. Wang, J. I. Ziegler, R. F. Haglund, S. T. Pantelides, and K. I. Bolotin, "Bandgap Engineering of Strained Monolayer and Bilayer MoS₂," *Nano Lett.*, vol. 13, pp. 3626-3630, 2013/08/14 2013.
- [89] Y. Wang, C. Cong, C. Qiu, and T. Yu, "Raman Spectroscopy Study of Lattice Vibration and Crystallographic Orientation of Monolayer MoS₂ under Uniaxial Strain," *Small*, vol. 9, pp. 2857-2861, 2013.
- [90] A. Castellanos-Gomez, R. Roldán, E. Cappelluti, M. Buscema, F. Guinea, H. S. J. van der Zant, and G. A. Steele, "Local Strain Engineering in Atomically Thin MoS₂," *Nano Lett.*, vol. 13, pp. 5361-5366, 2013/11/13 2013.

- [91] N. A. Lanzillo, A. Glen Birdwell, M. Amani, F. J. Crowne, P. B. Shah, S. Najmaei, Z. Liu, P. M. Ajayan, J. Lou, M. Dubey, S. K. Nayak, and T. P. Regan, "Temperature-dependent phonon shifts in monolayer MoS₂," *Appl. Phys. Lett.*, vol. 103, p. 093102, 2013.
- [92] S. Najmaei, Z. Liu, P. M. Ajayan, and J. Lou, "Thermal effects on the characteristic Raman spectrum of molybdenum disulfide (MoS₂) of varying thicknesses," *Appl. Phys. Lett.*, vol. 100, p. 013106, 2012.
- [93] R. Yan, J. R. Simpson, S. Bertolazzi, J. Brivio, M. Watson, X. Wu, A. Kis, T. Luo, A. R. Hight Walker, and H. G. Xing, "Thermal Conductivity of Monolayer Molybdenum Disulfide Obtained from Temperature-Dependent Raman Spectroscopy," *ACS Nano*, vol. 8, pp. 986-993, 2014/01/28 2013.
- [94] S. Najmaei, P. M. Ajayan, and J. Lou, "Quantitative analysis of the temperature dependency in Raman active vibrational modes of molybdenum disulfide atomic layers," *Nanoscale*, vol. 5, pp. 9758-9763, 2013.
- [95] A. Taube, J. Judek, C. Jastrzębski, A. Duzynska, K. Świtkowski, and M. Zdrojek, "Temperature-Dependent Nonlinear Phonon Shifts in a Supported MoS₂ Monolayer," *ACS Appl. Mater. interfaces*, vol. 6, pp. 8959-8963, 2014/06/25 2014.
- [96] C. Y. Ho, R. W. Powell, and P. E. Liley, "Thermal Conductivity of the Elements," *J. Phys. Chem. Ref. Data*, vol. 1, pp. 279-421, 1972.
- [97] J. Kang, W. Liu, and K. Banerjee, "High-performance MoS₂ transistors with low-resistance molybdenum contacts," *Appl. Phys. Lett.*, vol. 104, p. 093106, 2014.
- [98] H. Liu, K. Xu, X. Zhang, and P. D. Ye, "The integration of high-k dielectric on two-dimensional crystals by atomic layer deposition," *Appl. Phys. Lett.*, vol. 100, p. 152115, 2012.
- [99] H. Murrmann and D. Widmann, "Current crowding on metal contacts to planar devices," *IEEE Trans. Electron Devices*, vol. 16, pp. 1022-1024, 1969.
- [100] X.-L. Qi and S.-C. Zhang, "Topological insulators and superconductors," *Rev. Mod. Phys.*, vol. 83, pp. 1057-1110, 2011.
- [101] Y. L. Chen, J. G. Analytis, J.-H. Chu, Z. K. Liu, S.-K. Mo, X. L. Qi, H. J. Zhang, D. H. Lu, X. Dai, Z. Fang, S. C. Zhang, I. R. Fisher, Z. Hussain, and Z.-X. Shen, "Experimental Realization of a Three-Dimensional Topological Insulator, Bi₂Te₃," *Science*, vol. 325, pp. 178-181, July 10, 2009 2009.
- [102] Y. Xia, D. Qian, D. Hsieh, L. Wray, A. Pal, H. Lin, A. Bansil, D. Grauer, Y. S. Hor, R. J. Cava, and M. Z. Hasan, "Observation of a large-gap topological-insulator class

with a single Dirac cone on the surface," *Nature Phys.*, vol. 5, pp. 398-402, 06//print 2009.

[103] Z. Wang, R. L. J. Qiu, C. H. Lee, Z. Zhang, and X. P. A. Gao, "Ambipolar Surface Conduction in Ternary Topological Insulator $\text{Bi}_2(\text{Te}_{1-x}\text{Se}_x)_3$ Nanoribbons," *ACS Nano*, vol. 7, pp. 2126-2131, 2013/03/26 2013.

[104] C. H. Lee, R. He, Z. Wang, R. L. J. Qiu, A. Kumar, C. Delaney, B. Beck, T. E. Kidd, C. C. Chancey, R. M. Sankaran, and X. P. A. Gao, "Metal-insulator transition in variably doped $(\text{Bi}_{1-x}\text{Sbx})_2\text{Se}_3$ nanosheets," *Nanoscale*, vol. 5, pp. 4337-4343, 2013.

[105] D. Kim, S. Cho, N. P. Butch, P. Syers, K. Kirshenbaum, S. Adam, J. Paglione, and M. S. Fuhrer, "Surface conduction of topological Dirac electrons in bulk insulating Bi_2Se_3 ," *Nature Phys.*, vol. 8, pp. 459-463, Jun 2012.

[106] N. Bansal, N. Koirala, M. Brahlek, M.-G. Han, Y. Zhu, Y. Cao, J. Waugh, D. S. Dessau, and S. Oh, "Robust topological surface states of Bi_2Se_3 thin films on amorphous SiO_2/Si substrate and a large ambipolar gating effect," *Appl. Phys. Lett.*, vol. 104, p. 241606, 2014.

[107] M.-X. Wang, C. Liu, J.-P. Xu, F. Yang, L. Miao, M.-Y. Yao, C. L. Gao, C. Shen, X. Ma, X. Chen, Z.-A. Xu, Y. Liu, S.-C. Zhang, D. Qian, J.-F. Jia, and Q.-K. Xue, "The Coexistence of Superconductivity and Topological Order in the Bi_2Se_3 Thin Films," *Science*, vol. 336, pp. 52-55, April 6, 2012 2012.

[108] J. Zhang, C.-Z. Chang, P. Tang, Z. Zhang, X. Feng, K. Li, L.-l. Wang, X. Chen, C. Liu, W. Duan, K. He, Q.-K. Xue, X. Ma, and Y. Wang, "Topology-Driven Magnetic Quantum Phase Transition in Topological Insulators," *Science*, vol. 339, pp. 1582-1586, March 29, 2013 2013.

[109] M. Brahlek, N. Koirala, M. Salehi, N. Bansal, and S. Oh, "Emergence of Decoupled Surface Transport Channels in Bulk Insulating Bi_2Se_3 Thin Films," *Phys. Rev. Lett.*, vol. 113, p. 026801, 07/07/ 2014.

[110] R. He, Z. Wang, R. L. J. Qiu, C. Delaney, B. Beck, T. E. Kidd, C. C. Chancey, and X. P. A. Gao, "Observation of infrared-active modes in Raman scattering from topological insulator nanoplates," *Nanotechnology*, vol. 23, p. 455703, 2012.

[111] H. Zhu, C. A. Richter, E. Zhao, J. E. Bonevich, W. A. Kimes, H.-J. Jang, H. Yuan, H. Li, A. Arab, O. Kirillov, J. E. Maslar, D. E. Ioannou, and Q. Li, "Topological Insulator Bi_2Se_3 Nanowire High Performance Field-Effect Transistors," *Sci. Rep.*, vol. 3, p. 1757, 04/30/online 2013.

- [112] H. Li, H. Zhu, H. Yuan, L. You, C. A. Richter, J. J. Kopanski, E. Zhao, and Q. Li, "SnTe field effect transistors and the anomalous electrical response of structural phase transition," *Appl. Phys. Lett.*, vol. 105, p. 013503, 2014.
- [113] J. Hoffman, X. Pan, J. W. Reiner, F. J. Walker, J. P. Han, C. H. Ahn, and T. P. Ma, "Ferroelectric Field Effect Transistors for Memory Applications," *Adv. Mater.*, vol. 22, pp. 2957-2961, 2010.
- [114] H.-W. You and W.-J. Cho, "Charge trapping properties of the HfO₂ layer with various thicknesses for charge trap flash memory applications," *Appl. Phys. Lett.*, vol. 96, p. 093506, 2010.
- [115] H. Song, M. A. Reed, and T. Lee, "Single Molecule Electronic Devices," *Adv. Mater.*, vol. 23, pp. 1583-1608, 2011.
- [116] S. Yu and H.-S. P. Wong, "A Phenomenological Model for the Reset Mechanism of Metal Oxide RRAM," *IEEE Electron Device Lett.*, vol. 31, pp. 1455-1457, 2010.
- [117] A. Gerber, M. Fitsilis, R. Waser, T. J. Reece, E. Rije, S. Ducharme, and H. Kohlstedt, "Ferroelectric field effect transistors using very thin ferroelectric polyvinylidene fluoride copolymer films as gate dielectrics," *J. Appl. Phys.*, vol. 107, p. 124119, 2010.
- [118] M. Dawber, K. M. Rabe, and J. F. Scott, "Physics of thin-film ferroelectric oxides," *Rev. Mod. Phys.*, vol. 77, pp. 1083-1130, 10/17/ 2005.
- [119] C. M. Krowne, S. W. Kirchoefer, W. Chang, J. M. Pond, and L. M. B. Alldredge, "Examination of the Possibility of Negative Capacitance Using Ferroelectric Materials in Solid State Electronic Devices," *Nano Lett.*, vol. 11, pp. 988-992, 2011/03/09 2011.
- [120] A. G. Acosta, J. A. Rodriguez, and T. Nishida, "Mechanical stress effects on Pb(Zr,Ti)O₃ thin-film ferroelectric capacitors embedded in a standard complementary metal-oxide-semiconductor process," *Appl. Phys. Lett.*, vol. 104, p. 222908, 2014.
- [121] X. Zhu, Q. Li, D. E. Ioannou, D. Gu, J. E. Bonevich, H. Baumgart, J. S. Suehle, and C. A. Richter, "Fabrication, characterization and simulation of high performance Si nanowire-based non-volatile memory cells," *Nanotechnology*, vol. 22, p. 254020, 2011.
- [122] H. Zhu, J. E. Bonevich, H. Li, C. A. Richter, H. Yuan, O. Kirillov, and Q. Li, "Discrete charge states in nanowire flash memory with multiple Ta₂O₅ charge-trapping stacks," *Appl. Phys. Lett.*, vol. 104, p. 233504, 2014.
- [123] C.-H. Lee, K.-C. Park, and K. Kim, "Charge-trapping memory cell of SiO₂/SiN/high-k dielectric Al₂O₃ with TaN metal gate for suppressing backward-tunneling effect," *Appl. Phys. Lett.*, vol. 87, p. 073510, 2005.

[124] E. H. Nicollian and J. R. Brews, MOS (Metal Oxide Semiconductor) Physics and Technology. New York: Wiley, 1982

BIOGRAPHY

Hui Yuan received Bachelor of Engineering in Electronic Science and Technology and Master of Science in Condensed Matter Physics, both from Wuhan University, Wuhan, China, in 2006 and 2009, respectively. She has been working toward Ph.D. degree in the Department of Electrical and Computer Engineering, George Mason University, Fairfax, VA, since 2010. In the same time, she was a guest researcher in the Semiconductor and Dimensional Metrology Division at National Institute of Standards and Technology (NIST), Gaithersburg, MD. Her research interests include semiconductor nanowire FETs, two-dimensional semiconductor FETs and topological insulator devices. She has authored or co-authored 16 research papers in journals and conferences.

LIST OF PUBLICATIONS

Journal Publications

1. **H. Yuan**, A. Badwan, C. A. Richter, H. Zhu, O. Kirillov, D. E. Ioannou, and Q. Li, "Gate assisted Kelvin test structure to measure the electron and hole flows at the same nanowire contacts," *Appl. Phys. Lett.*, 105(13), 133513 (2014).
2. **H. Yuan**, Q. Li, H. Zhu, H. Li, D. Ioannou, and C. A. Richter, "Single-Nanowire CMOS Inverter Based on Ambipolar Si Nanowire FETs," *ECS Transactions* 50 (6), 151-156 (2013).
3. **H. Yuan**, G. Cheng, L. You, H. Li, H. Zhu, W. Li, J. J. Kopansiki, Y. S. Obeng, A. R. Hight Walker, D. J. Gundlach, C. A. Richter, D. E. Ioannou, and Q. Li, "Metal-MoS₂ Interface Influence on MoS₂ Transistors Performance: A Comparison of Ag and Ti Contacts," submitted to *ACS Appl. Mater. Interface*.
4. **H. Yuan**, K. Zhang, H. Li, H. Zhu, J. E. Bonevich, H. Baumgart, C. A. Richter, and Q. Li, "Polarization of Bi₂Te₃ Thin Film in a Floating-Gate Capacitor Structure," submitted to *Appl. Phys. Lett.*
5. **H. Yuan**, G. cheng, H. Li, H. Zhu, S. Yu, C. A. Richter, and Q. Li, "Gate Effects and Current Crowding in Metal/MoS₂ Contacts," to be submitted.
6. H. Li, H. Zhu, **H. Yuan**, L. You, C. A. Richter, J. J. Kopanski, E. Zhao, and Q. Li, "SnTe field effect transistors and the anomalous electrical response of structural phase transition," *Appl. Phys. Lett.* 105(1), 013503 (2014).
7. S. Yu, H. D. Xiong, K. Eshun, H. Yuan and Q. Li, "Phase transition, effective mass and carrier mobility of MoS₂ monolayer under tensile strain," *Appl. Surf. Sci.* Accepted 2014
8. H. Zhu, J. E. Bonevich, H. Li, C. A. Richter, **H. Yuan**, O. Kirillov, and Q. Li, "Discrete charge states in nanowire flash memory with multiple Ta₂O₅ charge-trapping stacks," *Appl. Phys. Lett.* 104(23), 233504 (2014).

9. H. Zhu, C. A. Richter, E. Zhao, J. E. Bonevich, W. A. Kimes, H. J. Jang, **H. Yuan**, H. Li, A. Arab, O. Kirillov, J. E. Masler, D. E. Ioannou, Q. Li, "Topological Insulator Bi₂Se₃ Nanowire High Performance Field-Effect Transistors," *Scientific Reports*, 3, 1757 (2013).
10. H. Zhu, **H. Yuan**, H. Li, C. Richter, O. Kirillov, and Q. Li, "Design and Fabrication of Tantalum Pentoxide Stacks for Discrete Multibit Memory Application," *IEEE Trans. Nanotechnol.* 12(6), 1151-1157 (2013).
11. H. Zhu, C. A. Hacker, S. J. Pookpanratana, C. A. Richter, **H. Yuan**, H. Li, O. Kirillov, D. E. Ioannou, and Q. Li, "Non-volatile memory with self-assembled ferrocene charge trapping layer," *Appl. Phys. Lett.* 103(5), 053102 (2013).
12. Q. Li, H. Zhu, **H. Yuan**, O. Kirillov, D. Ioannou, J. Suehle, and C. A. Richter, "A Study of Metal Gates on HfO₂ Using Si Nanowire Field Effect Transistors as Platform," *ECS Transactions*, 50(4), 267-271 (2013)
13. X. Liang, B. A. Sperling, I. Calizo, G. Cheng, C. A. Hacker, Q. Zhang, Y. Obeng, K. Yan, H. Peng, Q. Li, X. Zhu, **H. Yuan**, A. R. Hight Walker, Z. Liu, L. Peng, and C. A. Richter, "Toward Clean and Crackless Transfer of Graphene," *ACS Nano*, 5(11), 9144-9153 (2011).

Conferences and Presentations

1. **H. Yuan**, K. Zhang, H. Zhu, H. Li, D. E. Ioannou, H. Baumgart, C. Richter, and Q. Li, "Realization of Negative Capacitance with Topological Insulator Based MOS Capacitor," APS March Meeting, 2013
2. **H. Yuan**, Q. Li, H. Zhu, H. Li, D. E. Ioannou, and C. A. Richter, "Single-Nanowire CMOS Inverter based on Ambipolar Si Nanowire FETs," 2012 ECS Meeting.
3. **H. Yuan**, C. A. Richter, H. Zhu, H. Li, O. Kirillov, D. E. Ioannou, and Q. Li, "Measure the Electron and Hole Contact Resistance in Gated Kelvin Structure," Frontier of Characterization and Metrology for Nanoelectronics: 2013
4. **H. Yuan**, G. Cheng, L. You, H. Li, H. Zhu, W. Li, Y. S. Obeng, J. J. Kopanski, A. R. Hight Walker, D. Gundlach, C. A. Richter, D. E. Ioannou, and Q. Li, "Performance Enhancement of MoS₂ Field Effect Transistors with Silver Contacts," International Semiconductor Device Research Symposium 2013